JL7036C Datasheet

Zhuhai Jieli Technology Co.,LTD

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Revision History

Date	Revision	Description
2025.08.26	V1.0	Initial Release

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JL7036C Features

SYSTEM

- Dual Core 32bit DSP 320MHz
- With IEEE754 Single precision FPU
- Support FFT/MATRIX/MATH
- 2 x I-cache and D-cache
- Support SDTAP/EMU
- On-chip SRAM 528kbyte
- Support MMU
- Support MPU
- Support PSRAM
- Built-In Flash
- 24MHz crystal oscillator
- Internal RC oscillator,PLL

DSP Audio Processing

- Multi-MIC ENC
- Multi-band DRC
- Multi-band EQ

Audio

- 2 x 24bit DAC
  - SNR 109dB
  - Noise 5uVrms
  - Supports differential mode
  - Sampling rate 8~96kHz
- 3 x 24bit ADC
  - SNR 105dB
  - Sampling rate 8~48kHz
  - Support AMUX
- 2 x I^2S AUDIO Master/Slave interface
  - Sampling rate 8~384kHz
  - Support TX and RX
  - Support multi-slot mode(TDM)
- 1 x SPDIF AUDIO Master/Slave interface
  - Sampling rate 8~384kHz
  - Support TX and RX
- 1 x PDM AUDIO Slave interface
  - Sampling rate 8~192kHz
  - 2 x DMIC input

Peripherals

- 1 x High speed USB2.0
- 2 x SD host controller
- 6 x Multi-function 32bit timer
- 3 x UART interface
- 1 x I^2C Master/Slave interface
- 3 x SPI Master/Slave interface
- 3 x QDEC
- 1 x 10bit ADC(10 Channels)
- 20 x GPIO Support function remapping
- 1 x VLCD driver
- 3 x Light strip controller
- 12 x MCPWM
- 7 x LP_Touch with low power wake up
- 1 x IR RX

NFC

- NFC with low power wakeup

PMU

- Integrated battery charger up to 350mA
- Support temperature sensor
- VPWR range 4.5V to 5.5V
- VBAT range 2.7V to 4.5V
- IOVDD range 2.2V to 3.4V

Packages

- QFN32(4mm*4mm)

Temperature

- Operating temperature
  TC = -20℃ to +85℃(standard range)
  TC = -40℃ to +105℃(extended range)
- Storage temperature -65℃ to +150℃

Applications

- Audio DSP Products

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1 Block Diagram

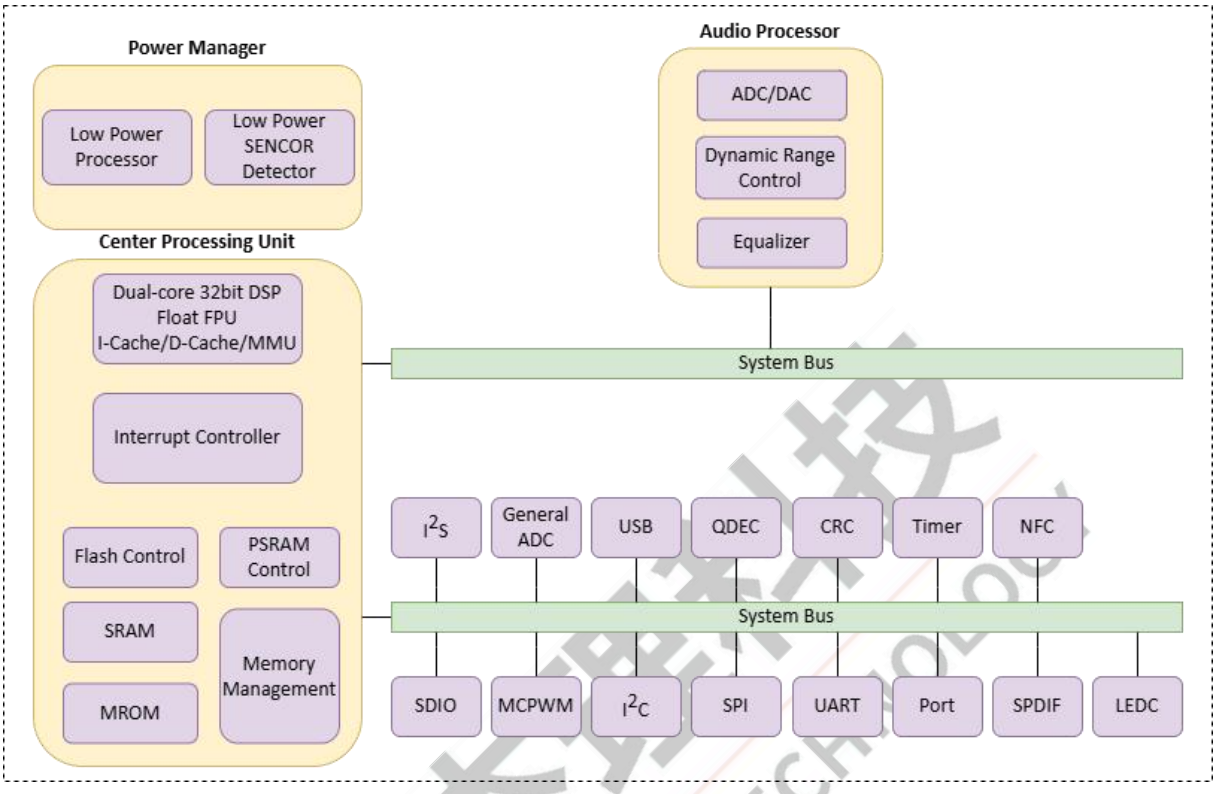


Figure 1-1 JL7036C Block Diagram

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2 Pin Definition

2.1 Pin Assignment

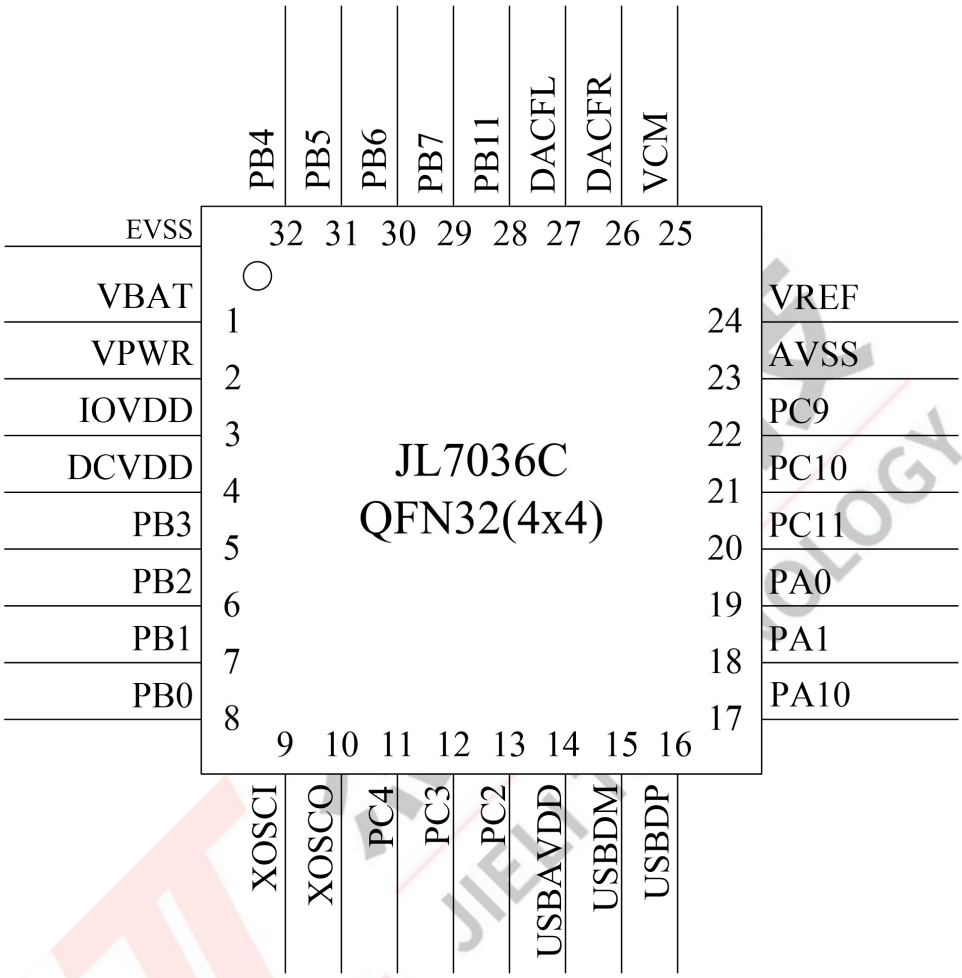


Figure 2-1 JL7036C Pin Assignment

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2.2 Pin Description

Table 2-2-1 JL7036C Pin Description

Pin No.	Name	Type	IO Initial State	Description
1	VBAT	P	--	Battery Input
2	VPWR	I/O	Z	Charge Power Input
3	IOVDD	P	--	IO Power
4	DCVDD	P	--	DCDC power
5	PB3	I/O	Z	ADC6(ADC Input Channel 6) LP_TOUCHA2(TOUCH_CHA2) NFC_TX
6	PB2	I/O	Z	LP_TOUCHA1(TOUCH_CHA1) NFC_RX
7	PB1	I/O	10kΩ Pull-up	Hold down 0 to reset ADC5(ADC Input Channel 5) LP_TOUCHA0(TOUCH_CHA0)
8	PB0	I/O	Z	--
9	XOSCI	I	--	Crystal Oscillator Input
10	XOSCO	O	--	Crystal Oscillator Output
11	PC4	I/O	Z	ADC13(ADC Input Channel 13) LCD COM1 PSRAM_CKA
12	PC3	I/O	Z	ADC12(ADC Input Channel 12) LCD COM2 PSRAM_CSA
13	PC2	I/O	Z	ADC11(ADC Input Channel 11) LCD COM3 LCD SEG18 PSRAM_D1A SPDIF_IN_AMP_D
14	USBAVDD	P	--	High Speed USB Power
15	USBDM	I/O	15kΩ Pull-down	USB Negative Data
16	USBDP	I/O	15kΩ Pull-down	USB Positive Data
17	PA10	I/O	Z	ADC3(ADC Input Channel 3) LCD SEG10 LCD_SPI_D3
18	PA1	I/O	Z	LCD SEG1 AIN_B2(Audio ADC Positive Input) MICBIASB(MIC Bias Output)

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Pin No.	Name	Type	IO Initial State	Description
19	PA0	I/O	Z	LCD SEG0 AIN_A2(Audio ADC Positive Input) MICBIASA(MIC Bias Output)
20	PC11	I/O	Z	LCD SEG24 AIN_C0N(Audio ADC Negative Input)
21	PC10	I/O	Z	LCD SEG23 AIN_C1(Audio ADC Positive Input) MICBIASC(MIC Bias Output)
22	PC9	I/O	Z	LCD SEG22 AIN_C0(Audio ADC Positive Input)
23	AVSS	G	--	Audio Ground
24	VREF	P	--	Audio Power
25	VCM	P	--	Audio Reference Voltage
26	DACFR	O	--	Front Right Channel DAC Output
27	DACFL	O	--	Front Left Channel DAC Output
28	PB11	I/O	Z	ADC10(ADC Input Channel 10) SD Power FM_TX_B
29	PB7	I/O	Z	LP_TOUCHB3(TOUCH_CHB3) AIN_A1(Audio ADC Positive Input)
30	PB6	I/O	Z	LP_TOUCHB2(TOUCH_CHB2) AIN_BN(Audio ADC Negative Input)
31	PB5	I/O	Z	LP_TOUCHB1(TOUCH_CHB1) LVD(External Low Voltage Detection Input) AIN_AN(Audio ADC Negative Input)
32	PB4	I/O	Z	LP_TOUCHB0(TOUCH_CHB0) ADC7(ADC Input Channel 7)

Note

1.IO initial state abbreviations Z--High resistance, H--High level, L--Low level, X--May be changed during power on.

2.Timer, MCPWM, QDEC, UART, LEDC, I^2C, I^2S, SPI,IR RX and SD functions can be remapped to any I/O.

3.PC6 input can not be Low in power on.

Table 2-2-2 Pin Types Description

Pin Type	Description	Pin Type	Description
P	Power	I/O	Input or Output
G	Ground	I	Input
RF	RF antenna	O	Output

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3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
Topt	Operating temperature	-20	+85	℃
Tstg	Storage temperature	-65	+150	℃
VBAT	Supply Voltage	-0.3	4.5	V
VPWR		-0.3	6	V
IOVDD		-0.3	3.6	V
DCVDD		-0.3	1.4	V
USBAVDD		-0.3	3.6	V
GPIO	Input voltage of GPIO (except PB0)	-0.3	3.6	V
HVTIO	Input voltage of HVT-IO (PB0)	-0.3	6	V

Note

1.Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.

3.2 ESD Ratings

Table 3-2 ESD Ratings

Parameter	Typ	Test pin	Reference standard
Human Body Mode	±4kV	All pins	JEDEC EIA/JESD22-A114
Machine Mode	±400V	All pins	JEDEC EIA/JESD22-A115
Charge Device Model	±1kV	All pins	ANSI/ESDA/JEDEC JS-002-2022

3.3 PMU Characteristics

Table 3-3 PMU Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VBAT	Voltage Input	--	2.7	3.7	4.5	V
VPWR	Charger supply Voltage	--	4.5	5.0	5.5	V
Operating mode						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
IOVDD	Voltage output	VBAT = 4.2V, 10mA loading	--	3	--	V
	Loading current	IOVDD=3.0V@VBAT = 3.7V or VPWR=5V	--	--	300	mA
DCVDD	Voltage output	--	--	1.2	--	V
	Loading current	DCVDD=1.2V@IOVDD=3.0V on LDO mode	--	--	150	mA
Low Power mode						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IOVDD	Loading current	IOVDD=3.0V@VBAT = 3.7V	--	--	20	mA

3.4 Battery Charge

Table 3-4 Charger Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
VPWR	Charge Input Voltage	4.5	5	5.5	V
CV	CV Mode Voltage Accuracy	4.175	4.2	4.225	V
		4.325	4.35	4.375	V
CC	CC Mode Current	15	--	350	mA
I_{end}	End Of Charge Current	1.5	--	35	mA
V_{TrikI}	Trickle Charge Voltage	--	3	--	V

3.5 IO Characteristics

Table 3-5 IO Characteristics

Input Characteristics						
Symbol	**Parameter**	**Conditions**	**IO**	**Min**	**Max**	**Unit**
V_{IL}	Low-Level Input Voltage	IOVDD = 3.0V	PA0,PA1,PA10 PB0~PB7,PB11 PC2~PC4,PC9~PC11 USBDP USBDM VPWR	-0.3	1.4	V
V_{IH}	High-Level Input Voltage	IOVDD = 3.0V	PA0,PA1,PA10 PB1~PB7,PB11 PC2~PC4,PC9~PC11 USBDP USBDM	1.7	3.3	V
		IOVDD = 3.0V	PB0 VPWR	1.7	5.5	V
Output Characteristics						
Symbol	**Parameter**	**Conditions**	**IO**	**Typ**		**Unit**
$\lvert I_{OL} \rvert$	Output Current	IOVDD = 3.0V Voutput = 0.3V	PA0,PA1,PA10 PB1~PB7,PB11 PC2~PC4,PC9~PC11	2(HD=0) 8(HD=1) 26(HD=2) 50(HD=3)		mA
			PB0 USBDP USBDM	8		mA
			VPWR	2		mA

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| I_{OH} |	Output Current	IOVDD = 3.0V Voutput = 2.7V	PA0,PA1,PA10 PB1~PB7,PB11 PC2~PC4,PC9~PC11	2(HD=0) 8(HD=1) 26(HD=2) 50(HD=3)	mA
			PB0 USBDP USBDM	8	mA
			VPWR	2	mA
Internal Resistance Characteristics					
Symbol	**Parameter**	**Conditions**	**IO**	**Typ**	**Unit**
R_{pu}	Pull-up Resistance	IOVDD = 3.0V	PA0,PA1,PA10 PB0~PB7,PB11 PC2~PC4,PC9~PC11 VPWR	10k(PU=1) 100k(PU=2) 1M(PU=3)	Ω
			USBDP USBDM	1.5k(PU=1) 1k(PU=3)	Ω
R_{pd}	Pull-down Resistance	IOVDD = 3.0V	PA0,PA1,PA10 PB0~PB7,PB11 PC2~PC4,PC9~PC11 VPWR	10k(PD=1) 100k(PD=2) 1M(PD=3)	Ω
			USBDP USBDM	15k(PD=1)	Ω

Note

1.Internal pull-up/pull-down resistance accuracy ±20%.

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3.6 Audio DAC Characteristics

Table 3-6 Stereo DAC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Resolution	--	--	--	24	bit
Output Sample Rate	--	8	--	96	kHz
SNR	Differential Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted load=10kΩ	--	109	--	dB
	Single-ended Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted load=10kΩ	--	106	--	dB
Dynamic Range	Differential Mode Fin=1kHz@-60dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted load=10kΩ	--	109	--	dB
	Single-ended Mode Fin=1kHz@-60dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted load=10kΩ	--	106	--	dB
THD+N	Differential Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted load=32Ω	--	-86	--	dB
	Single-ended Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted load=32Ω	--	-86	--	dB
Noise Floor	Differential Mode B/W=20Hz~20kHz A-Weighted load=10kΩ	--	7	--	uVrms
	Single-ended Mode B/W=20Hz~20kHz A-Weighted load=10kΩ	--	5	--	uVrms
Stereo Crosstalk	Single-ended Mode	--	-108	--	dB

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	Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted load=10kΩ				
Max Output Power	Differential Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted load=16Ω THD+N＜0.1%	--	30	85	mW
	Single-ended Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted load=16Ω THD+N＜0.1%	--	30	38	mW

3.7 Audio ADC Characteristics

Table 3-7 Audio ADC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Resolution	--	--	--	24	bits
Input Sample Rate	--	8	--	48	kHz
SNR	Differential input Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=-3dB	--	105	--	dB
	Single-ended input Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=-3dB	--	102	--	dB
Dynamic Range	Differential input Mode Fin=1kHz@-60dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=-3dB	--	105	--	dB
	Single-ended input Mode Fin=1kHz@-60dBFS Fs=44.1kHz	--	102	--	dB

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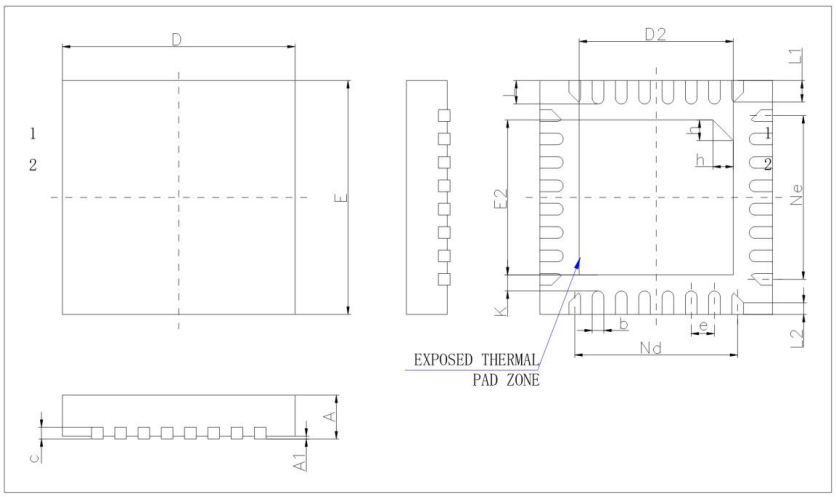
Parameter	Conditions	Min	Typ	Max	Unit
	B/W=20Hz~20kHz A-Weighted ADC gain=-3dB				
THD+N	Differential input Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=-3dB	--	-90	--	dB
	Single-ended input Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted ADC gain=-3dB	--	-90	--	dB
Analogue Gain	--	-9	--	32	dB
Max Input Level	Differential input Mode ADC gain=-3dB	--	2	--	Vrms
	Single-ended input Mode ADC gain=-3dB	--	1	--	Vrms

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4 Package Information

4.1 QFN32_4x4mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.65	0.80	0.95
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.50	2.65	2.80
e	0.40BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.50	2.65	2.80
Ne	2.80BSC		
K	0.20	-	-
L	0.35	0.40	0.45
L1	0.30	0.35	0.40
L2	0.15	0.20	0.25
h	0.30	0.35	0.40
L/F 载体尺寸 (mil)	112*112		

Figure 4-1 JL7036C Package

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5 IC Marking Information

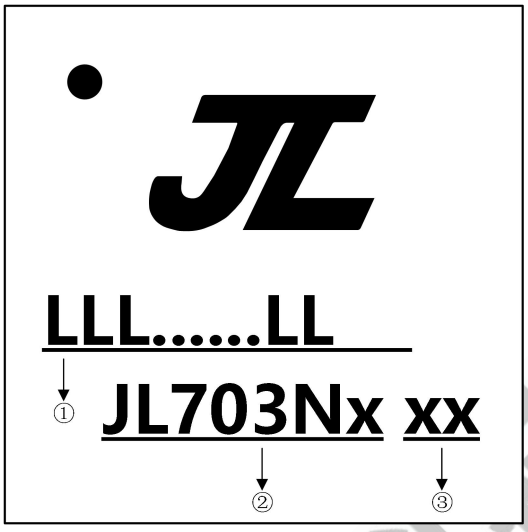


Figure 5-1 JL7036C Package Outline

① LLL……LL LOT No. , It contains 7 to 18 alphanumerics

② JL703Nx Chip Model

③ x Built-in flash size

0 No Flash Memory

2 2Mbit Flash

4 4Mbit Flash

8 8Mbit Flash

6 16Mbit Flash

3 32Mbit Flash

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6 Solder-Reflow Condition

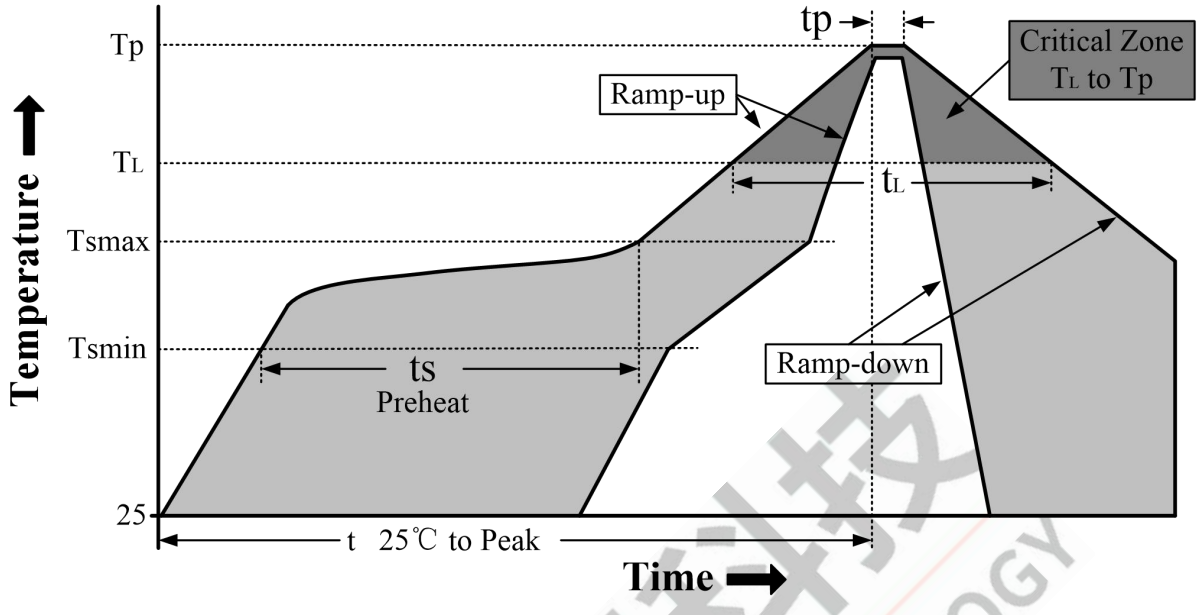


Figure 6-1 Classification Reflow Profile

Table 6-1 Classification Profiles

Profile Feature		Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak	Temperature Min (T_{smin})	100℃	150℃
	Temperature Max (T_{smax})	150℃	200℃
	Time (ts) from (T_{smin} to T_{smax})	60-120 seconds	60-180 seconds
Average ramp-up rate (T_{smax} to T_p)		3℃/second max	3℃/second max
Liquidous temperature (T_L) Time (t_L) maintained above T_L		183℃ 60-150 seconds	217℃ 60-150 seconds
Peak package body temperature (T_p)		See Table 6-2	See Table 6-3
Time within 5℃ of actual Peak Temperature (tp)[2]		10-30 seconds	20-40 seconds
Ramp-down rate (T_p to T_L)		6℃/second max	6℃/second max
Time 25℃ to peak temperature		6 minutes max	8 minutes max

Note

1.All temperatures refer to topside of the package, measured on the package body surface

2.Time within 5℃ of actual peak temperature (tp) specified for the reflow profiles is a "supplier" and "user" maximum.

Table 6-2 SnPb Classification Temperature

Package Thickness	Volume mm^3 < 350	Volume mm^3 ≥ 350
<2.5 mm	240 +0/-5℃	225 +0/-5℃
≥2.5 mm	225 +0/-5℃	225 +0/-5℃

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Table 6-3 Pb-free - Classification Temperature

Package Thickness	Volume mm^3 < 350	Volume mm^3 350 - 2000	Volume mm^3 > 2000
< 1.6mm	260℃	260℃	260℃
1.6 mm - 2.5mm	260℃	250℃	245℃
> 2.5mm	250℃	245℃	245℃

Note

1.*Tolerance The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0℃.For example 260℃+0℃)at the rated MSL level.

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