

AC6351D Datasheet

Zhuhai Jieli Technology Co.,LTD

Version: V2.0

Date: 2025.01.09

Copyright © Zhuhai Jieli Technology Co.,LTD. All rights reserved.

AC6351D Features

CPU

- 32-bit DSP supports hardware Float Point Unit(FPU)
- Up to 240MHz programmable processor
- 64Vectored interrupts
- 4 Levels interrupt priority

DSP Audio Processing

- SBC, AAC Audio decodes supported for BT audio
- mSBC voice codecs supported for BT phone
- Supports MP2, MP3, WMA, APE, FLAC, AAC, MP4, M4A, WAV, AIF, AIFC audio decoding
- Packet Loss Concealment (PLC) for voice processing
- Acoustic echo cancellation/suppression (AEC,AES)
- Single/Dual MIC Environmental Noise Cancellation (ENC)
- Multi-band DRC limiter
- 30-band EQ configuration for voice Effects

Audio Codec

- Two channels 16-bit DAC, SNR >= 92dB
- Three channels 16-bit ADC , SNR >= 90dB
- Sampling rates of 8KHz/11.025KHz/16KHz/22.05KHz/24KHz/32KHz/44.1KHz/48KHz are supported
- One analog MIC amplifier, build-in MIC bias generator
- Supports two PDM digital MIC inputs
- three channels Stereo analog MUX
- Supports cap-less, single-ended, and differential mode at the DAC path
- Supports 16ohm and 32ohm Speaker loading

Bluetooth

- Dual-mode BT6.0 (DN Q334307)
- Meet class1 class2 and class3 transmitting

power requirement

- Support GFSK and $\pi/4$ DQPSK all paket types
- Provides +6dbm transmitting power
- receiver with -90dBm sensitivity
- Fast AGC for enhanced dynamic range
- Supports a2dp\avctp\avdtp\avrcp\hfp\spp\smp\att\gap\gatt\rfcomm\sdpl2cap profile

Peripherals

- One full speed USB 2.0 OTG controller
 - Two PCM/IIS for external digital Audio code, supports host and device mode
 - Four multi-function 16-bit timers, support capture and PWM mode
 - Three 16-bit PWM generator for motor driving
 - Three full-duplex basic UART, UART0 and UART1 supports DMA mode
 - Three SPI interface supports host and device mode
 - Two SD Card Host controller
 - One hardwareIIC interface supports host and device mode
 - Four SPDIF receiving interface without analog amplify
 - Supports HDMI ARC (Audio Return Channel) receiving
 - Segment LCD panels
 - Digital matrix LED panels
 - Built-in Cap Sense Key controller
 - 14 channels 10-bit ADC for analog sampling
 - External wake up/interrupt on all GPIOs
- ## PMU
- Low voltage LDO for internal digital and analog circuit supply
 - 3uA current consumption in the soft-off mode
 - Built-in LDO for the core, I/O, Bluetooth and flash

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

- Built-inLi-Ion battery charger with up to 200mA charger current capability
- VBAT is 2.2V to 5.5V
- VDDIO is 2.2V to 3.6V

Packages

- LQFP48(7mm*7mm)

Temperature

- Operating temperature
TC=-20°C to +85°C (standard range)
TC=-40°C to +105°C (extended range)
- Storage temperature: -65°C to +150°C

Applications

- Bluetooth Keyboard

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

1、 Pin Definition

1.1 Pin Assignment

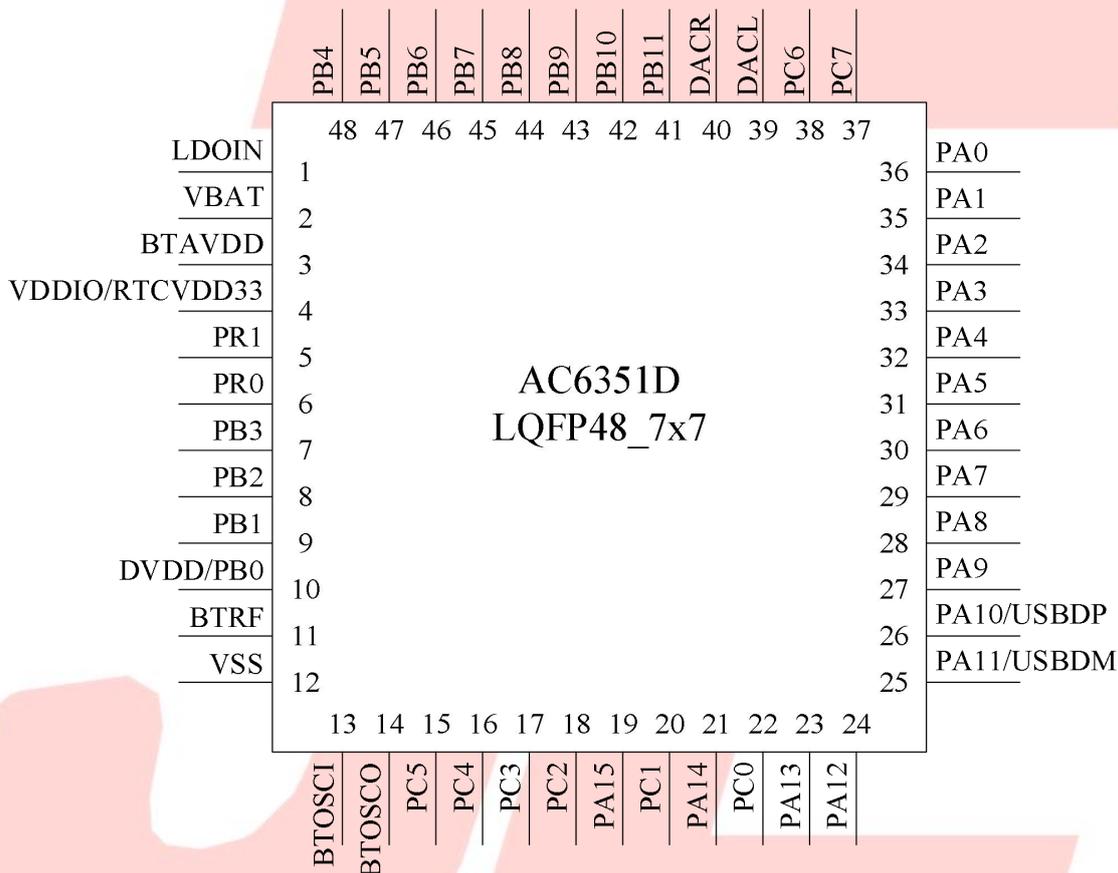


Figure 1-1 AC6351D_LQFP48 Package Diagram

1.2 Pin Description

Table 1-1 AC6351D_LQFP48 Pin Description

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
1	LDOIN	P	/		Battery Charger Power In;
2	VBAT	P	/		Power Supply;
3	BTA VDD	P	/		BT Power;
4	VDDIO	P	/		IO Power 3.3V;
	RTC VDD33	P	/		RTC Power;
5	PR1	I/O	8	GPIO	OSCO_32K: 32KHz OSC Out;
6	PR0	I/O	8	GPIO	OSCI_32K: 32KHz OSC In;
7	PB3	I/O	24/8	GPIO	PWM2: Timer2 PWM Output; ADC6: ADC Input Channel 6;
8	PB2	I/O	8	GPIO (High Voltage Resistance)	PWMCH1L: Motor PWM Channel1 (L);
9	PB1	I/O	24/8	GPIO (pull up)	Long Press Reset; ADC5: ADC Input Channel 5; UART1RXA: Uart1 Data In(A);
10	PB0	I/O	8	GPIO (High Voltage Resistance)	UART1TXA: Uart1 Data Out(A); PWMCH1H: Motor PWM Channel1 (H);
	DVDD	P	/		Core Power 1.2V;
11	BTRF	/	/		BT Antenna;
12	VSS	P	/		Ground;
13	BTOSCI	I	/		BT OSC In;
14	BTOSCO	O	/		BT OSC Out;
15	PC5	I/O	24/8	GPIO	SD1CLKA: SD1 Clock(A); SPI1DOB: SPI1 Data Out(B); UART2RXD: Uart2 Data In(D); IIC_SDA_B: IIC SDA(B); ADC13: ADC Input Channel 13; Touch15: Touch Input Channel 15; PWMCH5L: Motor PWM Channel5(L);

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

16	PC4	I/O	24/8	GPIO	SD1CMDA: SD1 Command(A); SPI1CLKB: SPI1 Clock(B); UART2TXD: Uart2 Data Out(D); IIC_SCL_B: IIC SCL(B); ADC10: ADC Input Channel 10; Touch14: Touch Input Channel 14; PWMCH5H: Motor PWM Channel5(H);
17	PC3	I/O	24/8	GPIO	SD1DAT0A: SD1 Data0(A); SPI1DIB: SPI1 Data In(B); Touch13: Touch Input Channel 13;
18	PC2	I/O	24/8	GPIO	SD1DAT1A: SD1 Data1(A); Touch12: Touch Input Channel 12; FPIN5: Motor Auto-Stop Protective Pin5;
19	PA15	I/O	24/8	GPIO	CAP2: Timer2 Capture;
20	PC1	I/O	24/8	GPIO	SD1DAT2A: SD1 Data2(A); Touch11: Touch Input Channel 11; UART1RXB: Uart1 Data In(B); FPIN4: Motor Auto-Stop Protective Pin4;
21	PA14	I/O	24/8	GPIO	FPIN0: Motor Auto-Stop Protective Pin0;
22	PC0	I/O	24/8	GPIO	SD1DAT3A: SD1 Data3(A); Touch10: Touch Input Channel 10; UART1TXB: Uart1 Data Out(B); FPIN3: Motor Auto-Stop Protective Pin3;
23	PA13	I/O	24/8	GPIO	
24	PA12	I/O	24/8	GPIO	PWM1: Timer1 PWM Output; ADC4: ADC Input Channel 4; UART0RXD: Uart0 Data In(D);
25	PA11	I/O	24/8	GPIO	UART0TXD: Uart0 Data Out(D);
	USBDM	I/O	4	USB Negative Data (pull down)	UART1RXD: Uart1 Data In(D); SPI2DOB: SPI2 Data Out(B); IIC_SDA_A: IIC SDA(A);
26	PA10	I/O	24/8	GPIO	SD0CLKA: SD0 Clock(A); ADC3: ADC Input Channel 3; TMR1: Timer1 Clock Input; Touch9: Touch Input Channel 9; UART2RXB: Uart2 Data In(B); PWMCH4L: Motor PWM Channel4(L);
	USBDP	I/O	4	USB Positive Data (pull down)	UART1TXD: Uart1 Data Out(D); SPI2CLKB: SPI2 Clock(B); IIC_SCL_A: IIC SCL(A); ADC12: ADC Input Channel 12;

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

27	PA9	I/O	24/8	GPIO	SD0CMA: SD0 Command(A); Touch8: Touch Input Channel 8; UART2TXB: Uart2 Data Out(B); PWMCH4H: Motor PWM Channel4(H);
28	PA8	I/O	24/8	GPIO	SD0DAT3A: SD0 Data3(A); FPIN2: Motor Auto-Stop Protective Pin2;
29	PA7	I/O	24/8	GPIO	SD0DAT2A: SD0 Data2(A); TMR0: Timer0 Clock Input; Touch7: Touch Input Channel 7;
30	PA6	I/O	24/8	GPIO	SD0DAT1A: SD0 Data1(A); ADC2: ADC Input Channel 2; IIC_SDA_D: IIC SDA(D); Touch6: Touch Input Channel 6; UART0RXA: Uart0 Data In(A);
31	PA5	I/O	24/8	GPIO	SD0DAT0A: SD0 Data0(A); ADC1: ADC Input Channel 1; IIC_SCL_D: IIC SCL(D); Touch5: Touch Input Channel 5; PWM0: Timer0 PWM Output; UART0TXA: Uart0 Data Out(A);
32	PA4	I/O	24/8	GPIO	Touch4: Touch Input Channel 4;
33	PA3	I/O	24/8	GPIO	Touch3: Touch Input Channel 3; UART2RXA: Uart2 Data In(A);
34	PA2	I/O	24/8	GPIO	Touch2: Touch Input Channel 2; UART2TXA: Uart2 Data Out(A); CAP3: Timer3 Capture;
35	PA1	I/O	24/8	GPIO	Touch1: Touch Input Channel 1; ADC0: ADC Input Channel 0; UART1RXC: Uart1 Data In(C); PWMCH0L: Motor PWM Channel0(L);
36	PA0	I/O	24/8	GPIO	Touch0: Touch Input Channel 0; CLKOUT0: Clk Out0; UART1TXC: Uart1 Data Out(C); PWMCH0H: Motor PWM Channel0(H);
37	PC7	I/O	/	GPIO	MIC BIAS: Microphone Bias Output;
38	PC6	I/O	/	GPIO	MIC: MIC Input Channel; ADC11: ADC Input Channel 11;
39	DACL	O	/		DAC Left Channel;
40	DACR	O	/		DAC Right Channel;
41	PB11	I/O	/	GPIO	SDPG:SDC Power Gate;

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

42	PB10	I/O	24/8	GPIO	SD0CMB: SD0 Command(B); SPI2DOA: SPI2 Data Out(A); SD1DAT3B: SD1 Data3(B); ADC9: ADC Input Channel 9; UART2RXC: Uart2 Data In(C); PWMCH3L: Motor PWM Channel3(L);
43	PB9	I/O	24/8	GPIO	SD0 Clock(B); SPI2CLKA: SPI2 Clk(A); SD1DAT2B: SD1 Data2(B); CAP0: Timer0 Capture; UART2TXC: Uart2 Data Out(C); PWMCH3H: Motor PWM Channel3(H);
44	PB8	I/O	24/8	GPIO	SD0DAT0B: SD0 Data0(B); SPI2_DIA: SPI2 Data In(A); SD1DAT1B: SD1 Data1(B); ADC8: ADC Input Channel 8; CLKOUT1: Clk Out1;
45	PB7	I/O	24/8	GPIO	
46	PB6	I/O	24/8	GPIO	SD1CLKB: SD1 Clock(B); SD0DAT1B: SD0 Data1(B); IIC_SDA_C: IIC SDA(C); TMR3: Timer3 Clock Input; UART0RXB: Uart0 Data In(B); PWMCH2L: Motor PWM Channel2 (L);
47	PB5	I/O	/	GPIO (High Voltage Resistance)	SD1CMDB: SD1 Command(B); SD0DAT2B: SD1 Data2(B); PWM3: Timer3 PWM Output; CAP1: Timer1 Capture; UART0TXC: Uart0 Data Out(C); UART0RXC: Uart0 Data In(C);
48	PB4	I/O	24/8	GPIO	SD1DAT0B: SD1 Data0(B); SD0DAT3B: SD0 Data3(B); IIC_SCL_C: IIC SCL(C); ADC7: ADC Input Channel 7; UART0TXB: Uart0 Data Out(B); LVD: Low Voltage Detect Input; PWMCH2H: Motor PWM Channel2 (H);

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

2、Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1

Symbol	Parameter	Min	Max	Unit
Tamb	Operating Temperature	-40	+85	°C
Tstg	Storage temperature	-65	+150	°C
VBAT	Supply Voltage	-0.3	4.5	V
LDOIN	Charger Voltage	-0.3	6	V
V _{3.3IO}	3.3V IO Input Voltage	-0.3	3.6	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

2.2 PMU Characteristics

Table 2-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VBAT	Voltage Input	2.2	3.7	4.5	V	-
LDOIN	Charger Voltage	4.5	5.0	5.5	V	-
V _{3.3}	Voltage output	2.2	3.0	3.4	V	VBAT = 3.7V, 100mA loading
V _{BT_AVDD}	Voltage output	1.2	1.25	1.35	V	VBAT = 3.7V, 100mA loading
I _{L3.3}	Loading current	-	-	150	mA	VBAT = 3.7V

2.3 IO Input/Output Electrical Logical Characteristics

Table 2-3

IO input characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{IL}	Low-Level Input Voltage	-0.3	-	0.3* VDDIO	V	VDDIO = 3.3V
V _{IH}	High-Level Input Voltage	0.7* VDDIO	-	VDDIO+0.3	V	VDDIO = 3.3V
IO output characteristics						
V _{OL}	Low-Level Output Voltage	-	-	0.33	V	VDDIO = 3.3V
V _{OH}	High-Level Output Voltage	2.7	-	-	V	VDDIO = 3.3V

2.4 Internal Resistor Characteristics

Table 2-4

Port	General Output	High Drive	Internal Pull-Up Resistor	Internal Pull-Down Resistor	Comment	
PA0~PA15 PB1, PB3, PB4 PB6~PB10 PC0~PC6	8mA	24mA	10K	10K	1、PB1 default pull up 2、USBDM & USBDP default pull down 3、PB0, PB2, PB5 can pull-up resistance to 5V 4、internal pull-up/pull-down resistance accuracy ±20%	
PB11 PC7	Output0	8mA	24mA	10K		10K
	Output1	8mA	64mA			
PB0, PB2, PB5	8mA	-	10K	10K		
PR0, PR1	8mA	-	10K	10K		
USBDP	4mA	-	1.5K	15K		
USBDM	4mA	-	180K	15K		

2.5 DAC Characteristics

Table 2-5

Parameter	Min	Typ	Max	Unit	Test Conditions
Frequency Response	20	-	20K	Hz	1KHz/0dB 10Kohm loading With A-Weighted Filter
THD+N	-	-75	-	dB	
S/N	-	92	-	dB	
Crosstalk	-	-80	-	dB	
Output Swing	-	1	-	Vrms	
Dynamic Range	-	90	-	dB	1KHz/-60dB 10Kohm loading With A-Weighted Filter
DAC Output Power	11	-	-	mW	32ohm loading

2.6 ADC Characteristics

Table 2-6

Parameter	Min	Typ	Max	Unit	Test Conditions
Dynamic Range	-	80	-	dB	1KHz/-60dB
S/N	-	90	91	dB	1KHz/-60dB
THD+N	-	-70	-	dB	
Crosstalk	-	-80	-	dB	

2.7 BT Characteristics

2.7.1 Transmitter

Basic Rate

Table 2-7

Parameter		Min	Typ	Max	Unit	Test Conditions
RF Transmit Power		-	4	6	dBm	25°C, Power Supply
RF Power Control Range		-	20	-	dB	
20dB Bandwidth		-	950	-	KHz	
In-band spurious Emissions (BQB Test Mode RF_Tx Power=4dBm)	F=F ₀ ±1MHz	-	-20	-	dBm	VBAT=3.7V 2441MHz DH5
	F=F ₀ ±2MHz	-	-45	-	dBm	
	F=F ₀ ±3MHz	-	-35	-	dBm	
	F=F ₀ ±>3MHz	-	-45	-	dBm	

Enhanced Data Rate

Table 2-8

Parameter		Min	Typ	Max	Unit	Test Conditions
Relative Power		-	-1	-	dB	25°C, Power Supply
π/4 DQPSK Modulation Accuracy	DEVM RMS	-	4	-	%	
	DEVM 99%	-	10	-	%	
	DEVM Peak	-	7	-	%	
In-band spurious Emissions (BQB Test Mode RF_Tx Power=4dBm)	F=F ₀ ±1MHz	-	-4	-	dBm	VBAT=3.7V 2441MHz 2DH5
	F=F ₀ ±2MHz	-	-30	-	dBm	
	F=F ₀ ±3MHz	-	-30	-	dBm	
	F=F ₀ ±>3MHz	-	-37	-	dBm	

2.7.2 Receiver

Basic Rate

Table 2-9

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity		-	-89	-	dBm	25°C, Power Supply VBAT=3.7V 2441MHz DH5
Co-channel Interference Rejection		-	7	-	dB	
Adjacent Channel selectivity C/I	+1MHz	-	-6	-	dB	
	-1MHz	-	-6	-	dB	
	+2MHz	-	-22	-	dB	
	-2MHz	-	-27	-	dB	
	+3MHz	-	-29	-	dB	
	-3MHz	-	-31	-	dB	

Enhanced Data Rate

Table 2-10

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity		-	-91	-	dBm	25°C, Power Supply VBAT=3.7V 2441MHz 2DH5
Co-channel Interference Rejection		-	9	-	dB	
Adjacent Channel selectivity C/I	+1MHz	-	-13	-	dB	
	-1MHz	-	-14	-	dB	
	+2MHz	-	-24	-	dB	
	-2MHz	-	-28	-	dB	
	+3MHz	-	-28	-	dB	
	-3MHz	-	-33	-	dB	

2.7.3 BLE

1M Data Rate

Table 2-11

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity		-	-93	-	dBm	25°C Power Supply VBAT=3.7V 2440MHz
RF Transmit Power		-	6.5	8	dBm	
In-band Spurious Emission	M-N =2MHz	-	-34	-	dBm	
	M-N ≥3MHz	-	-31	-	dBm	
Modulation Characteristics	Δf1 avg	-	250	-	KHz	
	Δf2 99%	-	210	-	KHz	
	Δf1avg/Δf2avg	-	0.9	-	/	
Carrier Frequency Offset		-15	-	+15	KHz	
Frequency Drift		-25	-	+25	KHz	
Frequency Drift Rate		-5	-	+5	KHz/50us	

2M Data Rate

Table 2-12

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity		-	-90	-	dBm	25°C Power Supply VBAT=3.7V 2440MHz
RF Transmit Power		-	6.5	8	dBm	
In-band Spurious Emission	M-N =4MHz	-	-40	-	dBm	
	M-N =5MHz	-	-40	-	dBm	
	M-N ≥6MHz	-	-40	-	dBm	
Modulation Characteristics	Δf1 avg	-	500	-	KHz	
	Δf2 99%	-	430	-	KHz	
	Δf1avg/Δf2avg	-	0.9	-	/	
Carrier Frequency Offset		-20	-	+20	KHz	
Frequency Drift		-25	-	+25	KHz	
Frequency Drift Rate		-5	-	+5	KHz/50us	

Long Range

Table 2-13

Parameter	Min	Typ	Max	Unit	Test Conditions
Sensitivity LE 125K(S8)	-	-100	-	dBm	VBAT=3.7V,25°C
Sensitivity LE 500K(S2)	-	-96	-	dBm	2440MHz

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

3、 Package Information

3.1 LQFP48(7mm*7mm)

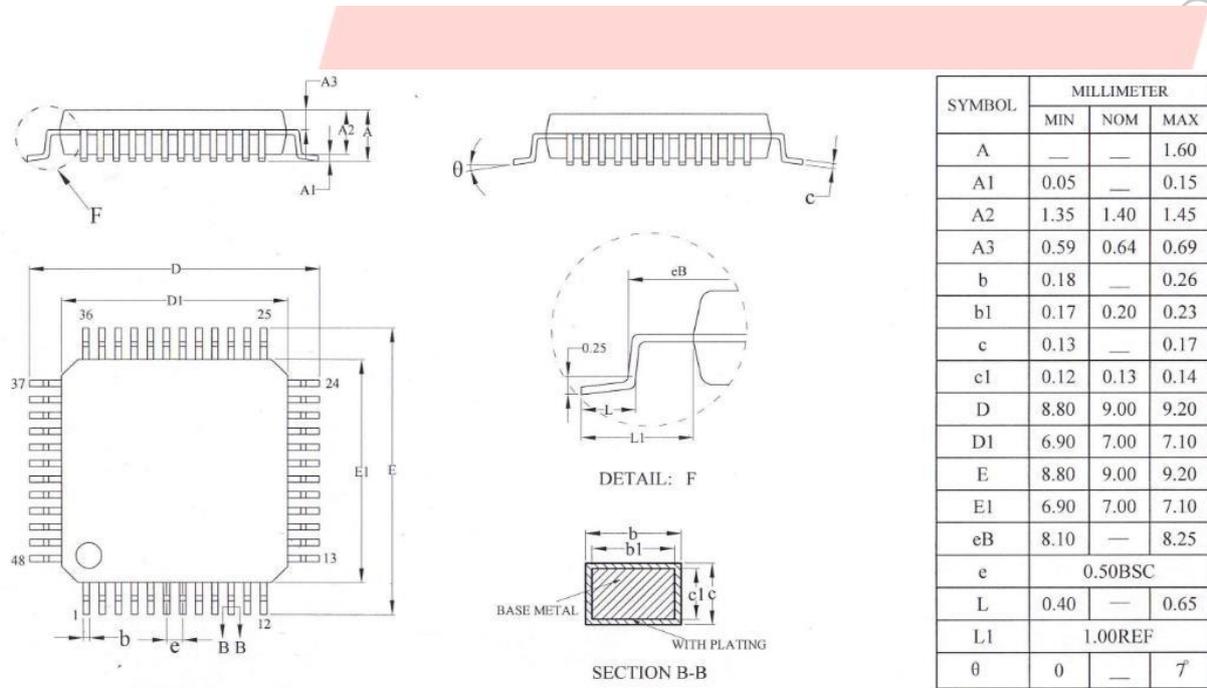


Figure 3-1. AC6351D_LQFP48 Package

4、Revision History

Date	Revision	Description
2020.08.11	V1.0	Initial Release
2022.07.19	V1.1	Update Bluetooth Feature
2024.03.06	V1.2	Update Bluetooth Feature, Add BLE Parameter
2024.06.27	V1.3	Update Pin Description, Add Audio Parameter
2025.01.09	V2.0	Update Bluetooth Feature