

JL7016G Datasheet

Zhuhai Jieli Technology Co.,LTD

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JL7016G Features

CPU

- 32bit Dual-Core DSP
- Maximum speed 160MHz
- 32KB ICache and 16KB DCache
- IEEE754 Single precision FPU
- Mathematical accelerate engine
- Interrupts with 8 priority level

Memory

- On-chip 640KB SRAM
- Support MMU
- Built-In Flash

Clocks

- On-chip 16 MHz clock oscillator
- On-chip 200 kHz lower-temperature-drift clock oscillator
- 24 MHz crystal oscillator

DSP Audio Processing

- SBC, AAC Audio decodes supported for BT audio
- mSBC voice codec supported for BT phone
- Supports MP2, MP3, WMA, APE, FLAC, AAC, MP4, M4A, WAV, AIF, AIFC audio decoding
- Packet Loss Concealment (PLC) for voice processing
- Single/Dual MIC Environmental Noise Cancellation (ENC)
- Multi-band DRC limiter
- Multi-band EQ configuration for voice Effects

Audio Codec

- Two channels 24-bit DAC, SNR \geq 104dB
- Four channels 24-bit ADC, SNR \geq 95dB
- Audio DAC Sampling rates of 8kHz/11.025kHz/16kHz/22.05kHz/24kHz/32kHz/44.1kHz/48kHz/64kHz/88.2kHz/96kHz are supported

- Audio ADC Sampling rates of 8kHz/11.025kHz/16kHz/22.05kHz/24kHz/32kHz/44.1kHz/48kHz are supported
- Support four digital/analog MIC inputs
- Four channels analog audio inputs
- Audio DAC support differential cap-less mode or single-ended mode
- Direct drive 16ohm/32ohm Speaker loading

ANC

- ANC processing engine up to 750 kHz sample rate
- 7.5 μ s analog to analog latency
- Supports 4 differential or single-ended analog inputs, 4 digital microphone inputs for ANC
- Supports 2 channels Feed-Forward, Feed-Back, Hybrid ANC
- ANC module include 20 double precision Biquad filters for each FF/FB/ music compensation control

Bluetooth

- Compliant with Bluetooth V5.3+BR+EDR+BLE specification
- Support AoA/AoD direction finding
- Support LE audio BIS/CIS full function
- Meet class2 and class3 transmitting power requirement
- Maximum +9dbm transmitting power
- EDR receiver with minimum -95dBm sensitivity
- Support a2dp\avctp\avdtp\avrcp\hfp\spp\smpl\att\gap\gatt\rfcomm\sdpl2cap profile
- bap 1.0\pac 1.0\ccp 1.0\mcp 1.0\micp 1.0\vep 1.0\csip 1.0
- a2dp 1.3.2\avctp 1.4\avdtp 1.3\avrcp 1.6.2\hfp 1.8\spp 1.2\rfcomm 1.1\pnp 1.3\hid 1.1.1\sdpl2cap core 5.3

Peripherals

- One full speed USB OTG controller
- One SD host controller for eMMC/SD
- Six multi-function 32-bit timers, support capture and PWM mode
- Four UART interface, UART0,UART1&UART2 support DMA
- I2C Master/Slave interface
- SPI Master/Slave interface
- I2S Master/Slave interface
- QDEC
- Low power CapSense
- 9-channel 10-bit ADC for analog sampling
- 4-channel Motor PWM controller
- 18 Individually programmable and multiplexed GPIO pins
- Up to 12 external interrupt/wake-up source(low power available,can be multiplexed to any I/O)

PMU

- Built-in lithium battery charging manager,up to 200mA charging current
- Built-in LDO and Buck DC-DC converter
- Less than 2uA sleep current
- VPWR range : 4.5V to 5.5V
- VBAT range : 2.2V to 4.5V
- IOVDD range : 2.2V to 3.6V

Packages

- QFN32(4mm*4mm)

Temperature

- Operating temperature: -40°C to +85°C
- Storage temperature: -65°C to +150°C

Applications

- Bluetooth TWS ANC Earphones
- Bluetooth TWS Earphones

1 Block Diagram

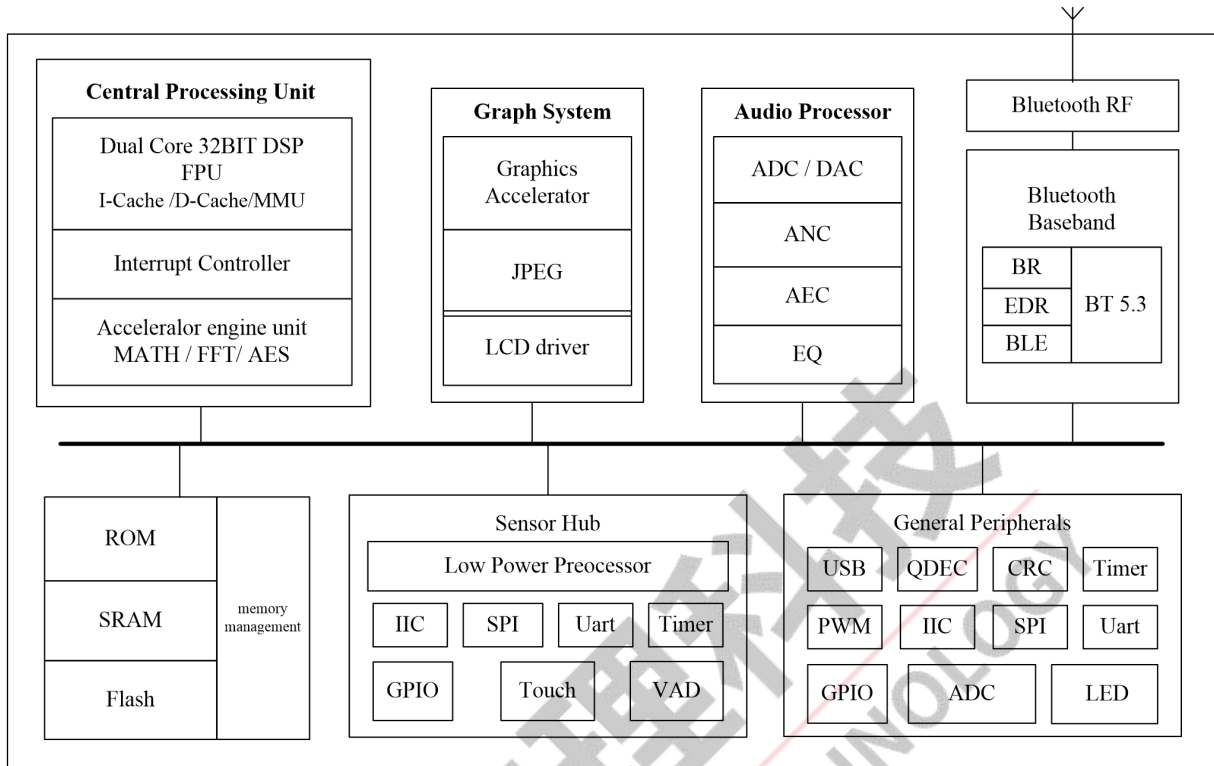


Figure 1-1 JL7016G Block Diagram

2 Pin Definition

2.1 Pin Assignments

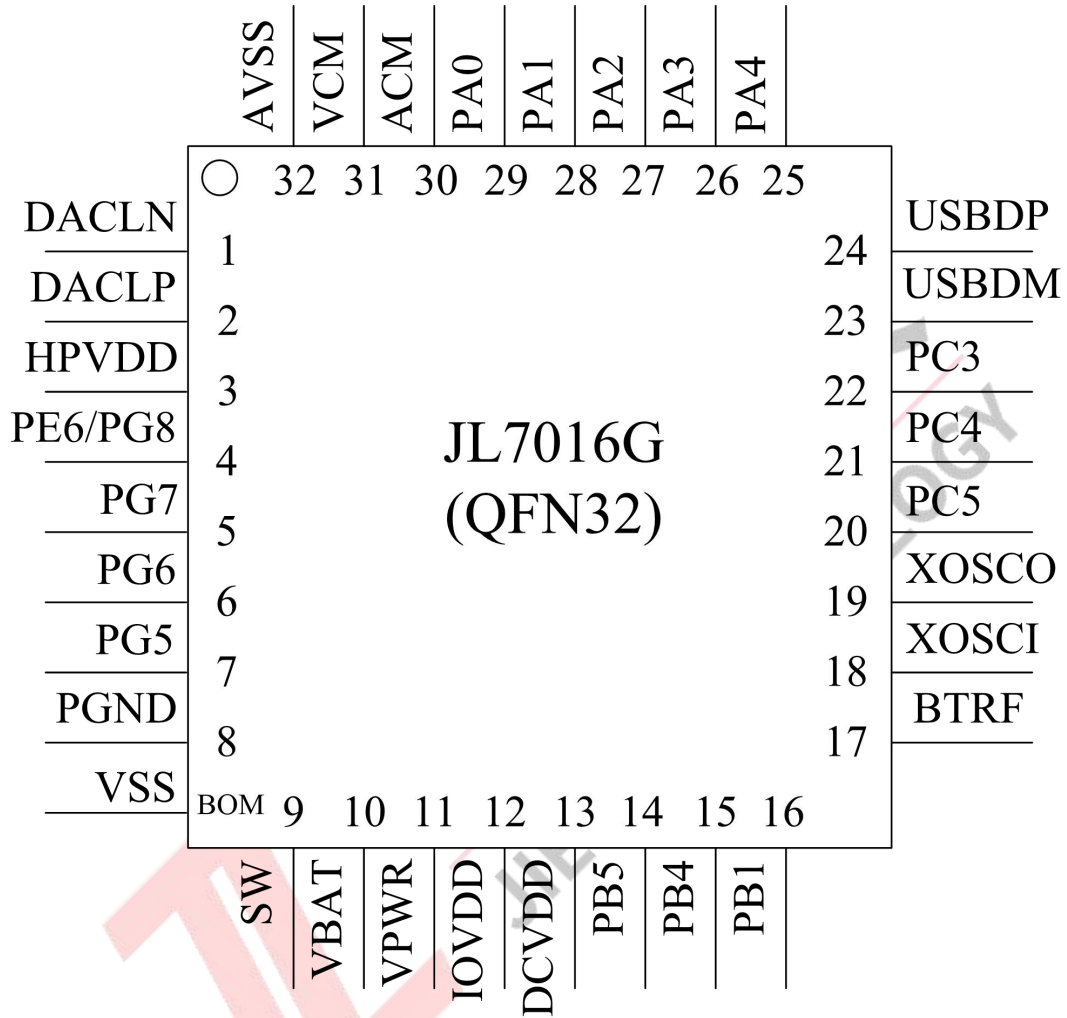


Figure 2-1 JL7016G Package Diagram

2.2 Pin Description

Table 2-1 JL7016G Pin Description

PIN NO.	Name	Type	Function	Other Function
1	DACLN	AO		Different DAC Left Negative Channel
2	DACL P	AO		Different DAC Left Positive Channel
3	HPVDD	PI		Audio power;
4	PE6	I/O	GPIO	SDPG: Supply Voltage to SD Card;
	PG8	I/O	GPIO	MICIN2: MIC2 Input Channel 2; MIC2_P: Different MIC2 Positive; AMUX_C0: Analog Channel C0 input;
5	PG7	I/O	GPIO	MIC_BIAS2: MIC2 Bias Output(Built-in resistor); MIC2_N: Different MIC2 Negative; AMUX_C1: Analog Channel C1 input; ADC15: ADC Input Channel 15;
6	PG6	I/O	GPIO	MICIN3: MIC3 Input Channel3; MIC3_P: Different MIC3 Positive; AMUX_D0: Analog Channel D0 input; FPIN2: Fault Detect In2;
7	PG5	I/O	GPIO	MIC_BIAS3: MIC3 Bias Output(Built-in resistor); MIC3_N: Different MIC3 Negative; AMUX_D1: Analog Channel D1 input; ADC14: ADC Input Channel 14; TMR3CK: PWM Timer3 CLK In;
8	PGND	G		The ground of Buck DC-DC converter;
9	SW	PO		Switch signal of the Buck converter,connected to Inductor;
10	VBAT	P		Battery interface;
11	VPWR (PP0)	PI (I/O)	GPIO (High Voltage Resistant)	Charging Power Input; UART0TXB: Uart0 Data Out(B); UART0RXB: Uart0 Data In(B); PWM3: Timer3 PWM Output; CAP1: Timer1 Capture;
12	IOVDD	PO		Built-in linear voltage regulator output;
13	DCVDD	P		Internal Power;
14	PB5	I/O	GPIO	LP_Touch4: Low Power Touch Channel 4; IIC1_SDA_A: IIC1 SDA(A); ADC8: ADC Input Channel 8; UART3RXB: Uart3 Data In(B);

15	PB4	I/O	GPIO	LP_Touch3: Low Power Touch Channel 3; CLKOUT0: Clock Out0; SPI4DIA: SPI4 Data In(A); IIC1_SCL_A: IIC1 SCL(A); UART3TXB: Uart3 Data Output(B); TMR2: Timer2 Clock Input;
16	PB1	I/O	GPIO	Hold down 0 to reset; LP_Touch1: Low Power Touch Channel 1; ADC6: ADC Input Channel 6;
17	BTRF	RFI		Bluetooth RF antenna interface;
18	XOSCI	I		System Crystal Oscillator Input;
19	XOSCO	O		System Crystal Oscillator Output;
20	PC5	I/O	GPIO	SPI0_DAT2C: SPI0 Data2(C); SD0_CLKA: SD0 Clock(A); SPI1DOB: SPI1 Data Out(B); IIC0_SDA_B: IIC0 SDA(B); ALNK_DAT3(B): Audio Link Data3(B); ADC5: ADC Input Channel 5; UART2RXA: Uart2 Data In(A);
21	PC4	I/O	GPIO	SPI0_DIC: SPI0 Data In(C); SD0CMDA: SD0 CMD(A); SPI1CLKB: SPI1 Clock(B); IIC0_SCL_B: IIC0 SCL(B); ALNK_DAT2B: Audio Link Data2(B); ADC4: ADC Input Channel 4; UART2TXA: Uart2 Data Out(A); PWM4: Timer4 PWM Output;
22	PC3	I/O	GPIO	SPI0_CSC: SPI0 Chip Select(C); SD0DATOA: SD0 Data Out(A); SPI1DIB: SPI1 Data In(B); ALNK_LRCKB: Audio Link Word Select(B); TMR3: Timer3 Clock Input;
23	USBDM	I/O	USB Negative Data (pull down)	SDTAP_DATB: SDTAP Data(B); SPI2DOB: SPI2 Data Out(B); IIC0_SDA_A: IIC0 SDA(A); ADC11: ADC Input Channel 11; UART1RXB: Uart1 Data In(B);
24	USBDP	I/O	USB Positive Data (pull down)	SDTAP_CLKB: SDTAP CLK(B); SPI2CLKB: SPI2 Clock(B); IIC0_SCL_A: IIC0 SCL(A); ADC10: ADC Input Channel 10; UART1TXB: Uart1 Data Out(B);

25	PA4	I/O	GPIO	MIC_BIAS1: MIC1 Bias Output(Built-in resistor); MIC1_N: Different MIC1 Negative; AMUX_B1: Analog Channel B1 input; SPI2DIA: SPI2 Data In(A); ALNK_DAT1A: Audio Link Data1(A); CAP2: Timer2 Capture;
26	PA3	I/O	GPIO	MICIN1: MIC1 Input Channel 1; MIC1_P: Different MIC1 Positive; AMUX_B0: Analog Channel B0 input; SPI1DOA: SPI1 Data Out(A); ALNK_DAT0(A): Audio Link Data0(A); PWM1: Timer1 PWM Output;
27	PA2	I/O	GPIO	MIC_BIAS0: MIC0 Bias Output(Built-in resistor); MIC0_N: Different MIC0 Negative; AMUX_A1: Analog Channel A1 input; CLKOUT1: Clock Out1; SPI1CLKA: SPI1 Clock(A); ALNK_MCLKA: ALNK Master Clock(A); UART1RXA: Uart1 Data In(A); CAP3: Timer3 Capture;
28	PA1	I/O	GPIO	MICIN0: MIC0 Input Channel 0; MIC0_P: Different MIC0 Positive; AMUX_A0: Analog Channel A0 input; SPI1DIA: SPI1 Data In(A); UART1TXA: Uart1 Data Out(A); PWM0: Timer0 PWM Output;
29	PA0	I/O	GPIO	MICLDO: MIC Power Supply; ADC0: ADC Input Channel 0;
30	ACM	P		Audio analog reference bias;
31	VCM	P		Audio analog reference bias;
32	AVSS	G		Audio analog ground;
PAD	VSS	G		System Ground;

Pin Type	Description	Pin Type	Description
P	Power	I/O	Input or Output
PO	Power Output	I	Input
PI	Power Input	O	Output
G	Ground	RFI	Radio frequency interface
AO	Analog Output		

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1

Symbol	Parameter	Min	Max	Unit
T _{opt}	Operating temperature	-40	+85	°C
T _{stg}	Storage temperature	-65	+150	°C
V _{BAT}	Supply Voltage	-0.3	4.5	V
V _{PWR}	Charger Voltage	-0.3	6	V
V _{IOVDD}	Voltage applied at IOVDD	-0.3	3.6	V
V _{GPIO}	Voltage applied to GPIO	-0.3	IOVDD+0.3	V
V _{HVIO}	Voltage applied to High Voltage Resistant IO	-0.3	+5.5	V
V _{HPVDD}	Voltage applied at HPVDD	-0.3	+3	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

3.2 PMU Characteristics

Table 3-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{BAT}	Voltage Input	2.2	3.7	4.4	V	
V _{PWR}	Charger supply Voltage	4.5	5.0	5.5	V	
Operating mode						
IOVDD	Voltage output	_	3.0	_	V	V _{BAT} = 4.2V, 10mA loading
	Loading current	_	_	200	mA	IOVDD=3.2V@V _{BAT} = 3.5V
DCVDD	Voltage output	_	1.25	_	V	IOVDD=3.0V, 10mA loading
	Loading current	_	_	100	mA	DCVDD=1.25V@IOVDD=3.0v on LDO mode
_		_	_	180	mA	DCVDD=1.25V@V _{BAT} =3.0v on DCDC mode
EVDD	Voltage output	_	1.1	_	V	DCVDD=1.25V, 1mA loading
	Loading current	_	_	5	mA	EVDD=1.1V@DCVDD=1.25v
Low Power mode						
IOVDD	Loading current	_	_	10	mA	IOVDD=3V@V _{BAT} = 4.2V

3.3 Battery Charge

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VPWR	Charge Input Voltage	4.5	5	5.5	V	–
V _{bat float}	Charge Voltage	4.15	4.2	4.25	V	VPWR > 4.5V
		4.30	4.35	4.40	V	VPWR > 4.65V
I _{bat}	Charge Current	15	–	200	mA	Charge current at fast charge mode VBAT=4.0V@VPWR=5.0V
I _{end}	End Of Charge Current	2	–	30	mA	End of charge current
V _{Trickl}	Trickle Charge Voltage	–	3.0	–	V	VPWR > 4.5V
I _{Trickl}	Trickle Charge Current	1.5	–	30	mA	V _{BAT} < V _{Trickl}

Table 3-3

3.4 IO Input/Output Electrical Logical Characteristics

Table 3-4

GPIO input characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{IL}	Low-Level Input Voltage	-0.3	–	0.3* IOVDD	V	IOVDD = 3.0V
V _{IH}	High-Level Input Voltage	0.7* IOVDD	–	IOVDD+0.3	V	IOVDD = 3.0V
High Voltage Resistant IO input characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{IL}	Low-Level Input Voltage	-0.3	–	0.3* IOVDD	V	IOVDD = 3.0V
V _{IH}	High-Level Input Voltage	0.7* IOVDD	–	+5V	V	IOVDD = 3.0V
GPIO & High Voltage Resistant IO output characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{OL}	Low-Level Output Voltage	–	–	0.1* IOVDD	V	IOVDD = 3.0V
V _{OH}	High-Level Output Voltage	0.9* IOVDD	–	–	V	IOVDD = 3.0V

3.5 Internal Resistor Characteristics

Table 3-5

Port	Drive(mA)		Internal Pull-Up Resistor	Internal Pull-Down Resistor	Comment
PA0~PA4	HD,HD0==0,0	2.4	10K	10K	1、PB1 default pull up 2、USBDM & USBDP default pull Down 3、internal pull-up / pull-down resistance accuracy $\pm 20\%$
PC3~PC5	HD,HD0==0,1	8			
PG5~PG8	HD,HD0==1,0	26			
PE6	HD,HD0==1,1	46			
PP0(VPWR) PB1~PB5	8		10K	10K	
USBDP	4		1.5K	15K	
USBDM			180K	15K	

3.6 DAC Characteristics

Table 3-6

Parameter	Min	Typ	Max	Unit	Audio Format	Test Conditions
Frequency Response	20	–	20k	Hz	–	Differential Mode 1KHz/0dB
Output Swing	–	1	–	Vrms	–	
THD+N	–	-77	–	dB	PCM	32 ohm loading With A-Weighted Filter
	–	-70	–	dB	SBC	
S/N	–	105	–	dB	PCM	
	–	105	–	dB	SBC	
Dynamic Range	–	104	–	dB	PCM	Differential Mode 1KHz/-60dB 32 ohm loading With A-Weighted Filter
	–	104	–	dB	SBC	
Noise Floor	–	5.6	–	uVrms	–	A-Weighted Filter
DAC Output Power	–	32	–	mW	–	Differential Mode 32ohm loading

3.7 ADC Characteristics

Table 3-7

Parameter	Min	Typ	Max	Unit	Test Conditions
Dynamic Range		94		dB	Fsample=44.1kHz, Gain=0dB Fin=1KHz 590mVrms
SNR	–	95	–	dB	Fsample=44.1kHz, Gain=0dB Fin=1KHz 590mVrms
THD+N	–	-75	–	dB	
SNR	–	76	–	dB	Fsample=44.1kHz, Gain=18dB Fin=1KHz 75mVrms
THD+N	–	-73	–	dB	

3.8 BT Characteristics

3.8.1 Transmitter

Basic Data Rate

Table 3-8

Parameter	Min	Typ	Max	Unit	Test Conditions
RF Transmit Power		7	9	dBm	25°C, Power Supply VBAT=3.7V 2441MHz
RF Power Control Range		18		dB	
20dB Bandwidth		950		KHz	
In-band spurious	F=F ₀ ± 1MHz	-20		dBm	
Emissions	F=F ₀ ± 2MHz	-51		dBm	
(BQB Test Mode RF_Tx Power=5dBm)	F=F ₀ ± 3MHz	-55		dBm	
	F=F ₀ +/->3MHz	-55		dBm	

Enhanced Data Rate

Table 3-9

Parameter	Min	Typ	Max	Unit	Test Conditions
Relative Power		-2		dB	25°C, Power Supply VBAT=3.7V 2441MHz
π /4 DQPSK Modulation Accuracy	DEVm RMS	9		%	
	DEVm 99%	23		%	
	DEVm Peak	18		%	
In-band spurious Emissions (BQB Test Mode RF_Tx Power=5dBm)	F=F ₀ ± 1MHz	-4		dBm	
	F=F ₀ ± 2MHz	-34		dBm	
	F=F ₀ ± 3MHz	-43		dBm	
	F=F ₀ +/->3MHz	-48		dBm	

3.8.2 Receiver

Basic Data Rate

Table 3-10

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-92		dBm	25°C, Power Supply VBAT=3.7V 2441MHz DH5
Co-channel Interference Rejection			10		dB	
Adjacent channel selectivity C/I	+1MHz		-4		dB	
	-1MHz		-3		dB	
	+2MHz		-39		dB	
	-2MHz		-33		dB	
	+3MHz		-45		dB	
	-3MHz		-28		dB	

Enhanced Data Rate

Table 3-11

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity		-95	-94		dBm	25°C, Power Supply VBAT=3.7V 2441MHz 2DH5
Co-channel Interference Rejection			10		dB	
Adjacent channel selectivity C/I	+1MHz		-8		dB	
	-1MHz		-8		dB	
	+2MHz		-40		dB	
	-2MHz		-33		dB	
	+3MHz		-45		dB	
	-3MHz		-27		dB	

3.8.3 BLE

1M Data Rate

Table 3-12

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-96		dBm	25°C Power Supply VBAT=3.7V 2440MHz
RF Transmit Power			7		dBm	
In-band Spurious Emission	M-N =2MHz		-37		dBm	
	M-N ≥3MHz			-34	dBm	
Modulation Characteristics	Δf1 avg		250		KHz	
	Δf2 99%		211		KHz	
	Δf1avg/Δf2avg		0.9			
Carrier Frequency Offset		-15		+15	KHz	
Frequency Drift		-25		+25	KHz	
Frequency Drift Rate		-5		+5	KHz/50us	

2M Data Rate**Table 3-13**

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-94		dBm	25°C Power Supply VBAT=3.7V 2440MHz
RF Transmit Power			7		dBm	
In-band Spurious Emission	M-N =4MHz		-44		dBm	
	M-N =5MHz		-43		dBm	
	M-N ≥6MHz			-48	dBm	
Modulation Characteristics	Δf1 avg		500		KHz	
	Δf2 99%		428		KHz	
	Δf1avg/Δf2avg		0.9			
Carrier Frequency Offset		-20		+20	KHz	
Frequency Drift		-25		+25	KHz	
Frequency Drift Rate		-5		+5	KHz/50us	

Long Range**Table 3-14**

Parameter	Min	Typ	Max	Unit	Test Conditions
Sensitivity LE 125K(S8)		-104		dBm	VBAT=3.7V,25°C
Sensitivity LE 500K(S2)		-100		dBm	2440MHz

3.9 ESD Protection**Table 3-12**

Parameter	Typ.	Test pin	Reference standard
Human Body Mode	±4KV	All pins	JEDEC EIA/JESD22-A114
Machine Mode	±200V	All pins	JEDEC EIA/JESD22-A115
Charge Device Model	±1KV	All pins	JEDEC EIA/JESD22-C101F
Latch up	±200mA	All GPIO pins	JEDEC STANDARD NO.78E
	1.5xVopmax	All power pins	

Note : 1.5xVopmax = 1.5 times maximum operating voltage.

4 Package Information

4.1 QFN32_4.0x4.0

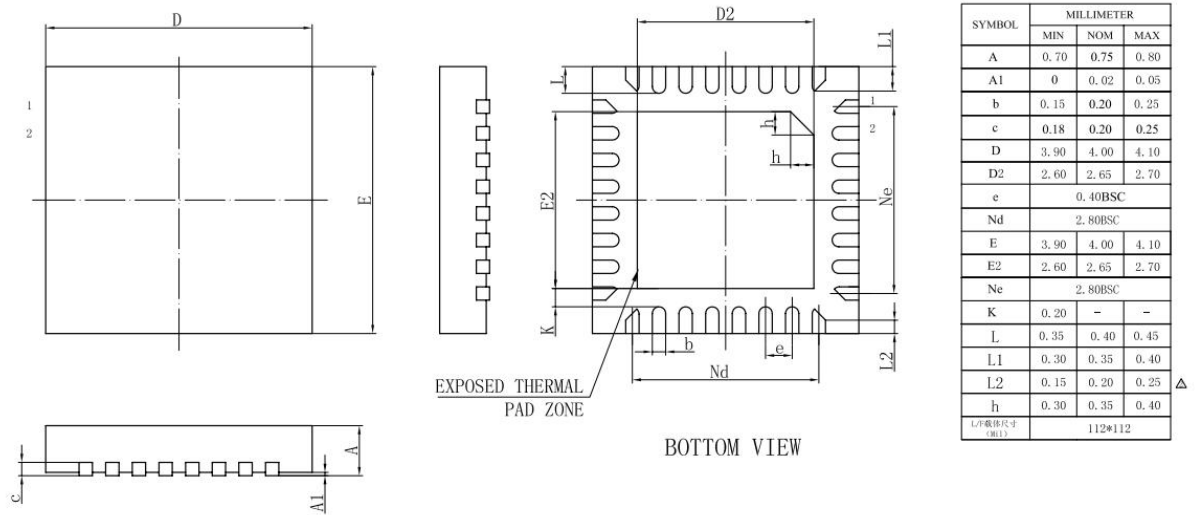
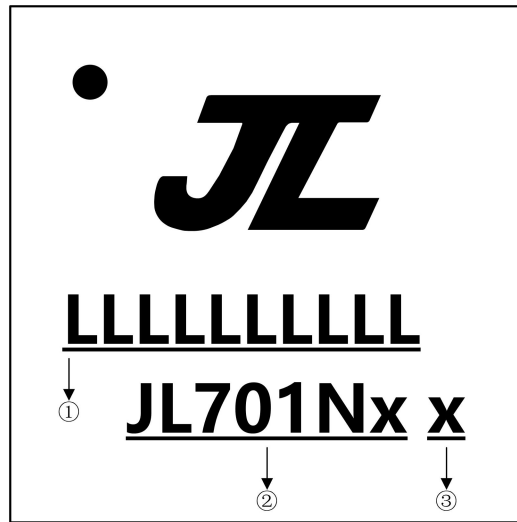


Figure 4-1 JL7016G Package

5 IC Marking Information



- ① LLLLLLLLLL: Production Batch
- ② JL701Nx: Chip Model
- ③ x: Built-in flash size
 - 0: No Flash Memory
 - 2: 2Mbit Flash
 - 4: 4Mbit Flash
 - 8: 8Mbit Flash
 - 6: 16Mbit Flash
 - 3: 32Mbit Flash

6 Solder-Reflow Condition

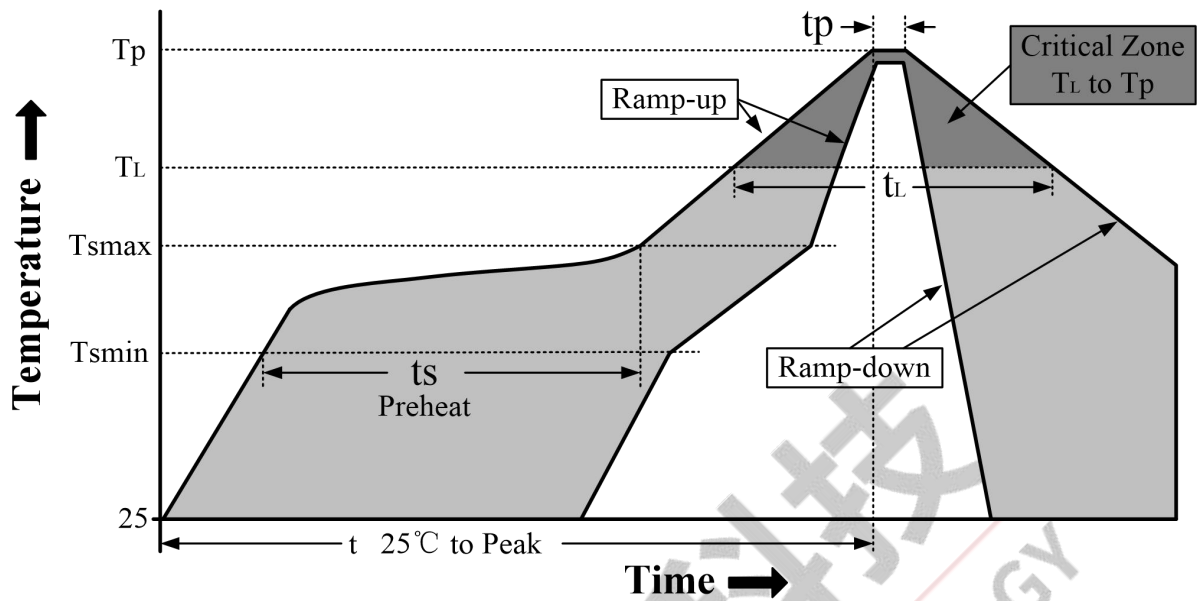


Figure 6-1 Classification Reflow Profile

Classification Profiles

Table 6-1

Profile Feature		Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/ Soak	Temperature Min (T_{smin})	100°C	150°C
	Temperature Max (T_{smax})	150°C	200°C
	Time (t_s) from (T_{smin} to T_{smax})	60-120 seconds	60-180 seconds
Average ramp-up rate (T_{smax} to T_p)		3°C/second max	3°C/second max
Liquidous temperature (T_L)		183°C	217°C
Time (t_L) maintained above T_L		60-150 seconds	60-150 seconds
Peak package body temperature (T_p)		See Table 6-2	See Table 6-3
Time within 5°C of actual Peak Temperature (t_p) ²		10-30 seconds	20-40 seconds
Ramp-down rate (T_p to T_L)		6°C/second max	6°C/second max
Time 25°C to peak temperature		6 minutes max	8 minutes max

Note 1: All temperatures refer to topside of the package, measured on the package body surface.

Note 2: Time within 5°C of actual peak temperature (t_p) specified for the reflow profiles is a “supplier” minimum and “user” maximum.

SnPb - Classification Temperature

Table 6-2

Package Thickness	Volume mm ³ < 350	Volume mm ³ ≥ 350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Pb-free - Classification Temperature**Table 6-3**

Package Thickness	Volume mm³ < 350	Volume mm³ 350 - 2000	Volume mm³ > 2000
< 1.6mm	260°C	260°C	260°C
1.6 mm - 2.5mm	260°C	250°C	245°C
> 2.5mm	250°C	245°C	245°C



7 Storage Condition

7.1 Moisture Sensitivity Level

JL7016G is qualified to moisture sensitivity level MSL3 in accordance with JEDEC J-STD-033.

7.2 Storage Alert

1. Calculated shelf life in sealed bag 12 months at $<40^{\circ}\text{C}$ and 90% relative humidity (RH).
2. Peak package body temperature $\leq 260^{\circ}\text{C}$.
3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be mounted within 168 hours of factory conditions $\leq 30^{\circ}\text{C}/60\%\text{RH}$ or stored per J-STD-033.
4. Devices require bake before mounting if humidity indicator card reads $> 10\%$ for level 2a-5a devices or $> 60\%$ for level 2 devices when read at $23 \pm 5^{\circ}\text{C}$, or 3a or 3b are not met.
5. Please refer to IPC/JEDEC J-STD-033 for baking procedure if necessary.

8 Revision History

Date	Revision	Description
2022.04.09	V1.0	Initial Release
2022.06.08	V1.1	Add Block Diagram & IC Marking Information & Solder-Reflow Condition
2022.09.20	V1.2	Add Storage Condition & Update IC Marking Information
2023.02.22	V1.3	Update Pin Description

