

AD176A Datasheet

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Version: 1.1

Date: 2023.09.28

AD176A Features

CPU

- 32bit DSP
- Maximum speed 160MHz
- Interrupts with 8 priority level

Memory

- Optional built-in flash memory

Clocks

- On-chip 16 MHz clock
- On-chip 200KHz lower-temperature-drift clock

Audio APA

- Support for driving 4 or 8 ohm speaker
- Mono Class-D Speaker Amplifier
 - 0.42W/8 Ω @3.7V
 - 0.17W/8 Ω @2.4V
 - 0.62W/4 Ω @3.7V
 - 0.25W/4 Ω @2.4V

Peripherals

- Three multi-function 16-bit timers, support capture and PWM mode
- Two UART Controllers(UART0/1) supports DMA and Flow Control
- One IIC Master controller
- Two SPI Master / Slaver controller with DMA

SPI0 support 4bit,SPI1 support 2bit

- 16-channel 10-bit general purpose ADC
- 4-channel Advance PWM controller
- 22 Individually programmable and multiplexed GPIO pins
- Digital peripheral crossbar
- Support Touch Key of pulse counter
- Up to 8 external interrupt / wake-up source (low power available,can be multiplexed to any I/O)
- Watchdog

PMU

- Less than 2uA soft off current
- VBAT range : 2.0V to 5.5V
- HPVDD range : 2.0V to 5.5V
- IOVDD range : 2.0V to 3.4V

Packages

- QFN32(4mm*4mm)

Temperature

- Operating temperature: -40°C to +85°C
- Storage temperature: -65°C to +150°C

Applications

- Sound Toy
- Audio player
- Universal Microcontroller

1 Block Diagram

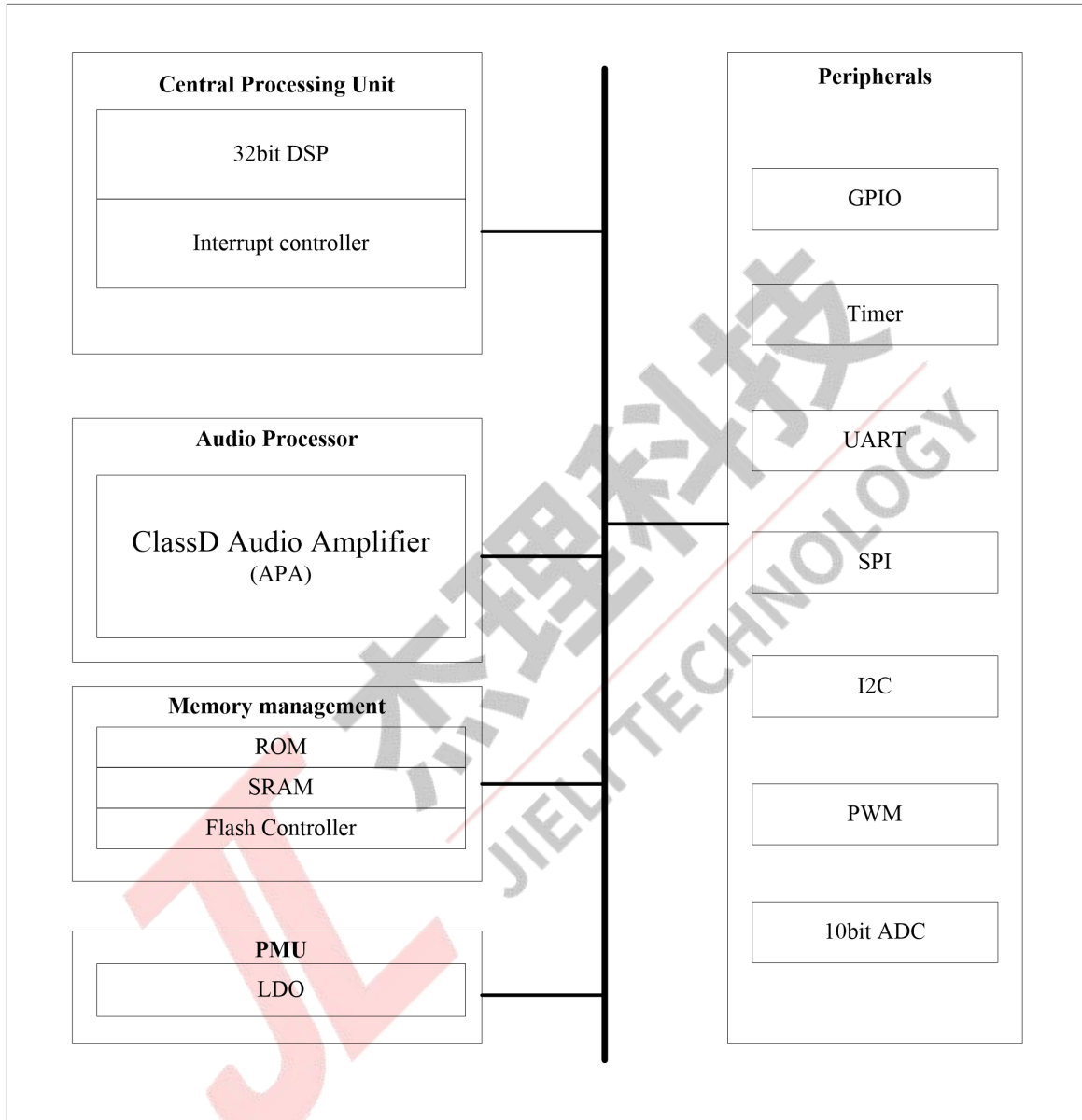


Figure 1-1 AD176A Block Diagram

2 Pin Definition

2.1 Pin Assignment

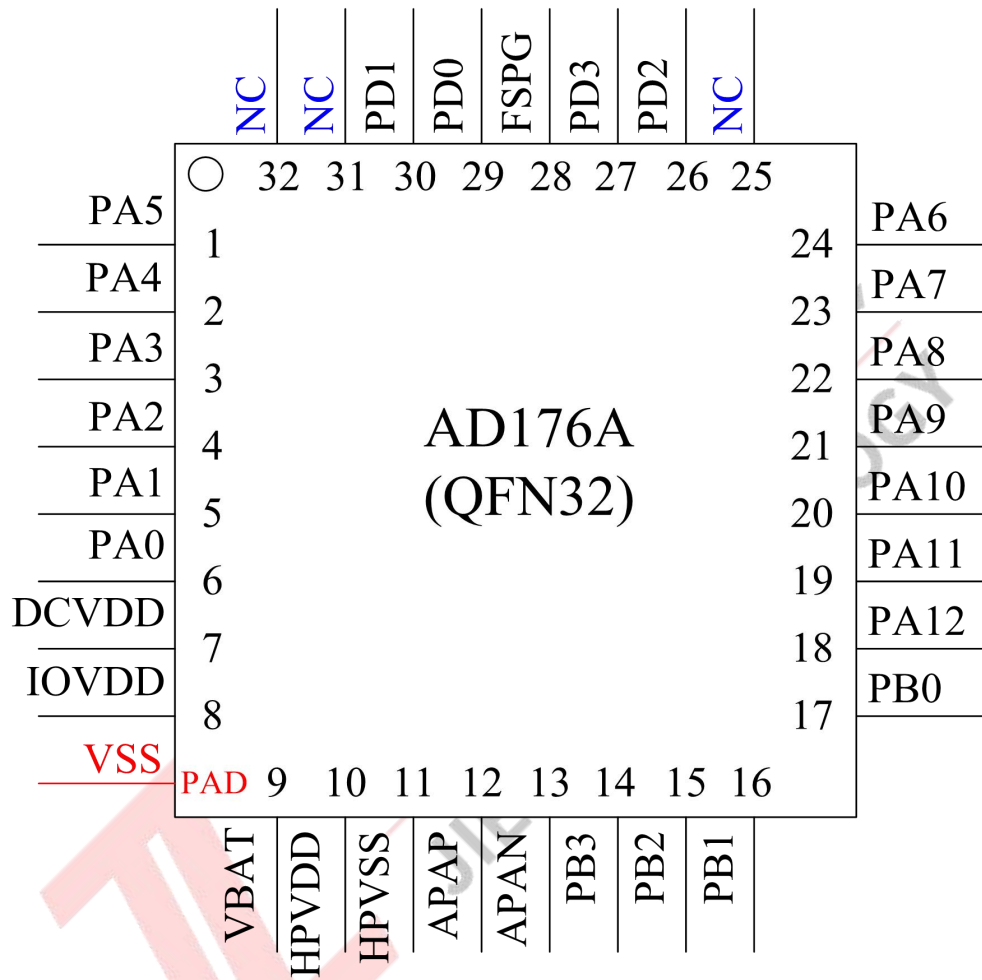


Figure 2-1 AD176A Package Diagram

2.2 Pin Description

Table 2-1 AD176A Pin Description

PIN NO.	Name	Type	Function	Other Function
1	PA5	I/O	GPIO	ADC5:ADC Input Channel 5; PWMCK1;
2	PA4	I/O	GPIO	ADC4:ADC Input Channel 4; PWMCK0;
3	PA3	I/O	GPIO	ADC3:ADC Input Channel 3; CAP0:Timer0 Capture; PWM0:Timer0 PWM Output;
4	PA2	I/O	GPIO	ADC2:ADC Input Channel 2; TMR0:Timer0 Clock Input;
5	PA1	I/O	GPIO	ADC1:ADC Input Channel 1; LVD:Low Voltage Detect;
6	PA0	I/O	GPIO (pull up)	Long press reset; ADC0:ADC Input Channel 0;
7	DCVDD	P		Internal Power
8	IOVDD	PO	Power supply for GPIO	Built-in linear voltage regulator output;
9	VBAT	PI		Power supply input;
10	HPVDD	PI		Class-D APA Power supply;
11	HPVSS	G		Class-D APA Ground;
12	APAP	O		Class-D APA Positive Output;
13	APAN	O		Class-D APA Negative Output;
14	PB3	I/O	5V tolerant IO	
15	PB2	I/O	5V tolerant IO (pull up)	MCLR:Low level reset;
16	PB1	I/O	5V tolerant IO	Serial port code upgrade pin;
17	PB0	I/O	5V tolerant IO	
18	PA12	I/O	GPIO	ADC12:ADC Input Channel 12;
19	PA11	I/O	GPIO	ADC11:ADC Input Channel 11;
20	PA10	I/O	GPIO	ADC10:ADC Input Channel 10;
21	PA9	I/O	GPIO (pull down)	ADC9:ADC Input Channel 9;
22	PA8	I/O	GPIO (pull down)	ADC8:ADC Input Channel 8;
23	PA7	I/O	GPIO (pull down)	ADC7:ADC Input Channel 7;
24	PA6	I/O	GPIO (pull down)	ADC6:ADC Input Channel 6;

25	NC			
26	PD2	I/O	GPIO	SFCCS:SFC Chip Select;
27	PD3	I/O	GPIO	SFCDI:SFC Data In; ADC14:ADC Input Channel 14;
28	FSPG	I/O	GPIO (pull down)	Flash Power Gate; ADC15:ADC Input Channel 15;
29	PD0	I/O	GPIO	SFCCLK:SFC Clk;
30	PD1	I/O	GPIO	SFCDO:SFC Data Out; ADC13:ADC Input Channel 13;
31	NC			
32	NC			
PAD	VSS	G		System ground;

Pin Type	Description	Pin Type	Description
P	Power	I/O	Input or Output
PI	Power Input	I	Input
PO	Power Output	O	Output
AO	Analog Output	G	Ground

CROSSBAR						
SPI0	SPI1	IIC	UART0	UART1	PWMCH0	PWMCH1
SPI0_CLK	SPI1_CLK	IIC_CLK	UART0_TX	UART1_TX	PWMCH0L	PWMCH1L
SPI0_DI	SPI1_DI	IIC_DAT	UART0_RX	UART1_RX	PWMCH0H	PWMCH1H
SP0_D0	SPI1_D0					
SP0_DAT2						
SP0_DAT3						

Input Channel x6			Output Channel x8		
WAKEUP	Timer1	IRFLT	PWM1	CLK_OUT0	APA_DOP
PWMFP0	Timer2	TOUCH_CAP	PWM2	CLK_OUT1	APA_DON
PWMFP1	CAP1	UART1_CTS	UART1_RTS	CLK_OUT2	
EXT_CLK	CAP2				

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1

Symbol	Parameter	Min	Max	Unit
Topt	Operating temperature	-40	+85	°C
Tstg	Storage temperature	-65	+150	°C
VBAT	Supply Voltage	-0.3	6	V
HPVDD	APA Power supplyVoltage	-0.3	6	V
V _{IOVDD}	Voltage applied at IOVDD	-0.3	3.6	V
V _{GPIO}	Voltage applied to GPIO	-0.3	IOVDD+0.3	V
V _{HVIO}	Voltage applied to High Voltage Resistant IO	-0.3	+5.5	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

3.2 ESD Protectio

Table 3-2

Parameter	Typ.	Test pin	Reference standard
Human Body Mode	±4KV	All pins	JEDEC EIA/JESD22-A114
Machine Mode	±200V	All pins	JEDEC EIA/JESD22-A115
Charge Device Model	±2KV	All pins	JEDEC EIA/JESD22-C101F
Latch up	±200mA	All GPIO pins	JEDEC STANDARD NO.78E
	1.5xVopmax	All power pins	

Note : 1.5xVopmax = 1.5 times maximum operating voltage.

3.3 PMU Characteristics

Table 3-3

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VBAT	Voltage Input	2.2	3.7	5.5	V	—
HPVDD	APA Power supplyVoltage	2.2	3.7	5.5	V	—
DCVDD	Voltage output	1.05	1.35	1.4	V	—
IOVDD	Voltage output	2.0	3.0	3.4	V	VBAT = 4.2V, 10mA loading
	Loading current	—	—	100	mA	IOVDD=3.3V@VBAT ≥ 3.6V
V _{LVD}	Voltage input	1.8	2.5	2.5	V	Low-Voltage Detection of IOVDD

3.4 IO Input/Output Electrical Logical Characteristics

Table 3-4

GPIO input characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{IL}	Low-Level Input Voltage	-0.3	-	0.3* IOVDD	V	IOVDD = 3.0V
V _{IH}	High-Level Input Voltage	0.7* IOVDD	-	IOVDD+0.3	V	IOVDD = 3.0V
High Voltage Resistant IO input characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{IL}	Low-Level Input Voltage	-0.3	-	0.3* IOVDD	V	IOVDD = 3.0V
V _{IH}	High-Level Input Voltage	0.7* IOVDD	-	+5V	V	IOVDD = 3.0V
Resistant IO output characteristics						
Symbol	Parameter	GPIO	Typ	Unit	Test Conditions	
V _{OL}	0.1*IOVDD Drive current	PA0~PA12 PD0~PD3	HD=1 : -7 HD=2 : -22 HD=3 : -27	mA	IOVDD = 3.0V	
		PB0~PB3	-7			
	0.1*HPVDD Drive current APA IO total current limit of 400mA	APAN APAP	-400		HPVDD=3.7V	
V _{OH}	0.9*IOVDD Drive current	PA0~PA12 PD0~PD3	HD=1 : 7 HD=2 : 24 HD=3 : 56	mA	IOVDD = 3.0V	
		PB0~PB3	7			
	0.9*HPVDD Drive current APA IO total current limit of 400mA	APAN APAP	400		HPVDD=3.7V	

3.5 Internal Resistor Characteristics

Table 3-5

Port	Internal Pull-Up Resistor	Internal Pull-Down Resistor	Comment
PA0~PA12,PB0~PB3,PD0~PD3	10K	200K	1. PA0,PB2 default pull up 2. PA6~PA9,FSPG default pull down 3. Internal pull-up/pull-down resistance accuracy ±20%

3.6 Audio APA Characteristics

Table 3-6

Parameter	MODE	Min	Typ	Max	Unit	Test Conditions		
Frequency Response		20	–	20K	Hz	R _L =10K, V _{BAT} =3.7V		
Output Swing	Diff (N to P)	–	1.57	–	V _{rms}	R _L =4Ω	f=1kHz/0dB V _{BAT} =3.7V	
		–	1.83	–	V _{rms}	R _L =8Ω		
		–	2.22	–	V _{rms}	R _L =10K		
	Single-ended	–	1.11	–	V _{rms}	R _L =10K		
	Diff (N to P)	–	0.99	–	V _{rms}	R _L =4Ω		f=1kHz/0dB V _{BAT} =2.4V
		–	1.17	–	V _{rms}	R _L =8Ω		
		–	1.44	–	V _{rms}	R _L =10K		
	Single-ended	–	0.72	–	V _{rms}	R _L =10K		
	Output power	Diff (N to P)	–	0.62	–	W	R _L =4Ω	
–			0.42	–	W	R _L =8Ω	V _{BAT} =3.7V	
–			0.25	–	W	R _L =4Ω	f=1kHz/0dB	
–			0.17	–	W	R _L =8Ω	V _{BAT} =2.4V	
THD+N	Diff (N to P)	–	-31	–	dB	R _L =4Ω	f=1kHz/0dB	
		–	-35	–	dB	R _L =8Ω	A-Weighted	
		–	-75	–	dB	R _L =10K	V _{BAT} =3.7V	
	Single-ended	–	-70	–	dB	R _L =10K		
	Diff (N to P)	–	-31	–	dB	R _L =4Ω	f=1kHz/0dB	
		–	-36	–	dB	R _L =8Ω	A-Weighted	
	Diff (N to P)	–	-73	–	dB	R _L =10K	V _{BAT} =2.4V	
Single-ended	–	-70	–	dB	R _L =10K			
S/N	Diff (N to P)	–	97	–	dB	R _L =4Ω	f=1kHz/0dB	
		–	97	–	dB	R _L =8Ω	A-Weighted	
		–	95	–	dB	R _L =10K	V _{BAT} =3.7V	
	Single-ended	–	75	–	dB	R _L =10K		
	Diff (N to P)	–	94	–	dB	R _L =4Ω	f=1kHz/0dB	
		–	94	–	dB	R _L =8Ω	A-Weighted	
	Diff (N to P)	–	88	–	dB	R _L =10K	V _{BAT} =2.4V	
Single-ended	–	72	–	dB	R _L =10K			
Dynamic Range	Diff (N to P)	–	88	–	dB	R _L =4Ω	f=1kHz/-60dB	
		–	88	–	dB	R _L =8Ω	A-Weighted	
		–	86	–	dB	R _L =10K	V _{BAT} =3.7V	
	Single-ended	–	75	–	dB	R _L =10K		
	Diff (N to P)	–	87	–	dB	R _L =4Ω	f=1kHz/-60dB	
		–	87	–	dB	R _L =8Ω	A-Weighted	
		–	85	–	dB	R _L =10K	V _{BAT} =2.4V	
	Single-ended	–	74	–	dB	R _L =10K		

4 Package Information

4.1 QFN32_4×4mm

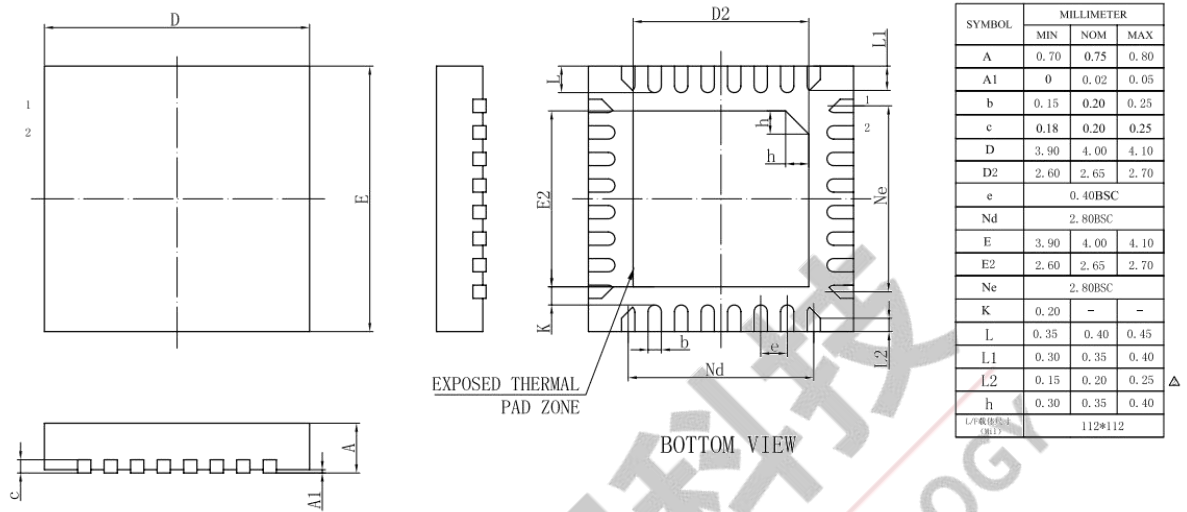
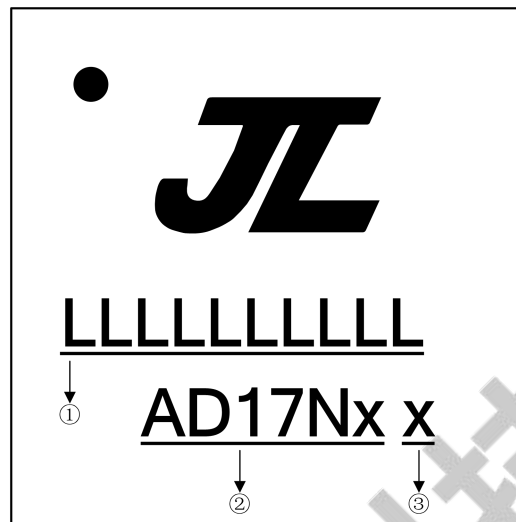


Figure 4-1 AD176A Package

5 IC Marking Information



① LLLLLLLLLL : Production Batch

② AD17Nx : Chip Model

③ Built-in flash size

0: No Flash Memory

2: 2Mbit Flash

4: 4Mbit Flash

8: 8Mbit Flash

6: 16Mbit Flash

3: 32Mbit Flash

6 Solder-Reflow Condition

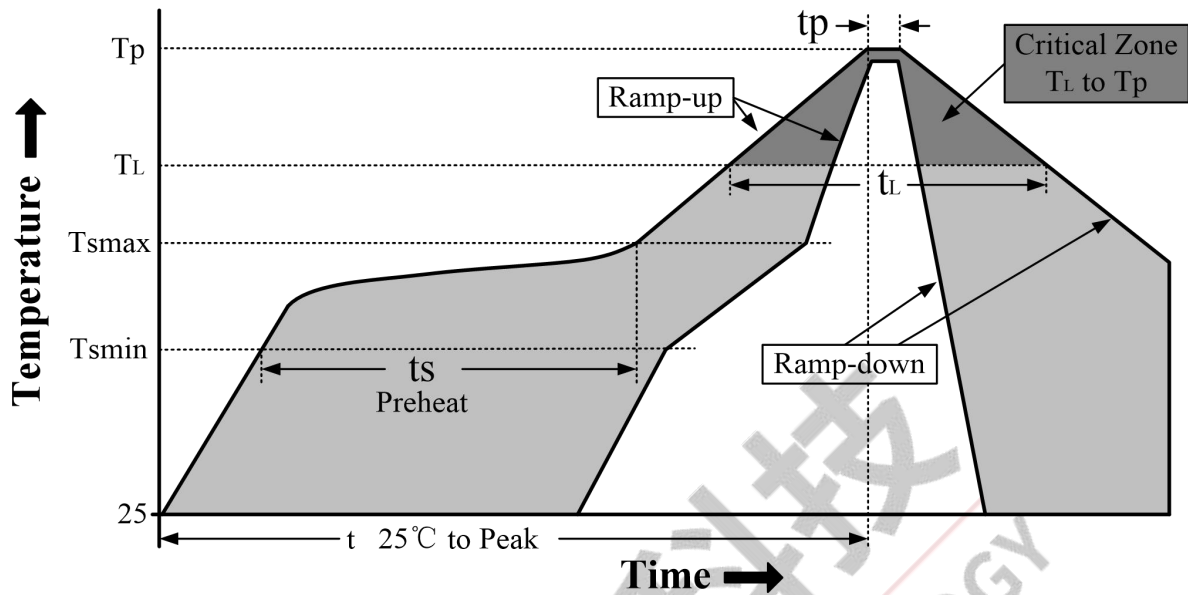


Figure 6-1 Classification Reflow Profile

Classification Profiles

Table 6-1

Profile Feature		Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/ Soak	Temperature Min (T_{smin})	100 °C	150 °C
	Temperature Max (T_{smax})	150 °C	200 °C
	Time (t_s) from (T_{smin} to T_{smax})	60-120 seconds	60-180 seconds
Average ramp-up rate (T_{smax} to T_p)		3 °C/second max	3 °C/second max
Liquidous temperature (T_L)		183 °C	217 °C
Time (t_L) maintained above T_L		60-150 seconds	60-150 seconds
Peak package body temperature (T_p)		See Table 6-2.	See Table 6-3.
Time within 5°C of actual Peak Temperature (t_p)		10-30 seconds	20-40 seconds
Ramp-down rate (T_p to T_L)		6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature		6 minutes max.	8 minutes max.

Note 1: All temperatures refer to topside of the package, measured on the package body surface.

Note 2: Time within 5°C of actual peak temperature (t_p) specified for the reflow profiles is a “supplier” minimum and “user” maximum.

SnPb - Classification Temperature

Table 6-2

Package Thickness	Volume mm^3 < 350	Volume mm^3 ≥ 350
<2.5 mm	240 +0/-5 °C	225 +0/-5 °C
≥ 2.5 mm	225 +0/-5 °C	225 +0/-5 °C

Pb-free - Classification Temperature **Table 6-3**

Package Thickness	Volume mm³ < 350	Volume mm³ 350 - 2000	Volume mm³ > 2000
< 1.6mm	260 °C	260 °C	260 °C
1.6 mm - 2.5mm	260 °C	250 °C	245 °C
> 2.5mm	250 °C	245 °C	245 °C



7 Revision History

Date	Revision	Description
2023.07.05	V1.0	Initial Release.
2023.09.28	V1.1	Update Pin Definition. Update Features modification.

