

AC6905A 芯片规格书

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AC6905A Features

High performance 32-bit RISC CPU

- RISC 32bit CPU
- DC-160MHz operation
- Support DSP instructions
- 64Vectored interrupts
- 4 Levels interrupt priority

Flexible I/O

- 9 GPIO pins
- All GPIO pins can be programmable as input or output individually
- All GPIO pins are internal pull-up/pull-down selectable individually
- CMOS/TTL level Schmitt triggered input
- External wake up/interrupt on all GPIOs

Peripheral Feature

- One full speed USB 2.0 OTG controller
- Four multi-function 16-bit timers, support capture and PWM mode
- One full-duplex basic UART
- One full-duplex advanced UART
- One SPI interface supports host and device mode
- Two SD Card Host controller
- One IIC interface supports host and device mode
- Watchdog
- 1 Crystal Oscillator
- 16-bit Stereo DAC, SNR > 90dB
- 1 channels Stereo ADC, SNR > 90dB
- 1 channel MIC amplifier
- Embedded headphone amplifier
- 1 channels Stereo analog MUX
- 10-bit ADC
- 2 channels 4 levels Low Voltage Detector
- Built in Cap Sense Key controller
- Power-on reset
- Embedded PMU

Bluetooth Feature

- CMOS single-chip fully-integrated radio and baseband
- Compliant with Bluetooth V4.2+BR+EDR+BLE specification
- Bluetooth Piconet and Scatternet support
- Meet class2 and class3 transmitting power requirement
- Provides +2dbm transmitting power
- receiver with -85dBm sensitivity
- Support a2dp\avctp\avdtp\avrcp\hfp\spp\smp\att\gap\gatt\rfcomm\sdp\l2cap profile

FM Tuner

- Support worldwide frequency band 76-108MHz
- Fully integrated digital low-IF tuner & frequency synthesizer
- Autonomous search tuning
- Digital auto gain control (AGC)
- Digital adaptive noise cancellation
- Programmable de-emphasis (50/75 uS)
- Receive signal strength indicator (RSSI)
- Digital volume control

Power Supply

- LDOIN is 3.3V to 5.5V
- VDDIO is 3.0V to 3.6V

Packages

- QSOP24

Temperature

- Operating temperature: -40°C to +85°C
- Storage temperature: -65°C to +150°C

一、引脚定义

1.1 引脚分配

<u>PC5</u>	1	AC6905A (QSOP24)	24	<u>BT_OSCO</u>
<u>PC4</u>	2		23	<u>BT_OSCI</u>
<u>USBDM/PC3</u>	3		22	<u>AVSS1</u>
<u>USB DP/PA4</u>	4		21	<u>BT_RF</u>
<u>PA3/PB13</u>	5		20	<u>AVSS2</u>
<u>DACR</u>	6		19	<u>BT_AVDD</u>
<u>DACL</u>	7		18	<u>LDO_IN</u>
<u>DACVDD</u>	8		17	<u>VSSIO</u>
<u>VCOM</u>	9		16	<u>PB9</u>
<u>FMIP</u>	10		15	<u>PB10</u>
<u>DACVSS</u>	11		14	<u>PB11</u>
<u>VDDIO</u>	12		13	<u>PB12</u>

图 1-1 AC6905A_QSOP24 引脚分配图

1.2 引脚描述

表 1-1 AC6905A_QSOP24 引脚描述

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
1	PC5	I/O	16	GPIO	SD1CLKA: SD1 Clk(A); PAPWR: PAP Write; SPI1DOB: SPI1 Data Out(B); UART2RXD: Uart2 Data In(D) IIC_SDA_B: IIC SDA(B);
2	PC4	I/O	16	GPIO	SD1CMDA: SD1 Command(A); SPI1CLKB: SPI1 Clk(B); UART2TXD: Uart2 Data Out(D); IIC_SCL_B: IIC SCL(B);
3	USBDM	I/O	4	USB Negative Data	
	PC3	I/O	16	GPIO	SD1DAT0A: SD1 Data0(A); SPI1DIB: SPI1 Data In(B); UART0RXC: Uart0 Data In(C)
4	USBDP	I/O	4	USB Positive Data	
	PA4	I/O	16	GPIO	AMUX1R: Simulator Channel1 Right; Touch11: Touch Input Channel 11; ADC1: ADC Input Channel 1; UART2RXA: Uart2 Data In(A); PWM1: Timer1 PWM Output;
5	PB13	I/O	16	GPIO	MIC
	PA3	I/O	16	GPIO	AMUX1L: Simulator Channel 1 Left; Touch10: Touch Input Channel 10; ADC0: ADC Input Channel 0; UART2TXA: Uart2 Data Out(A); Wakeup8: Port Interrupt /Wakeup 8;
6	DACR	O	/	DAC Right Channel	
7	DACL	O	/	DAC Left Channel	
8	DACVDD	P	/	DAC Power	
9	VCOM	P	/	DAC Reference	
10	FMIP	I	/		
11	DACVSS	P	/	DAC Ground	

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12	VDDIO	P	/	IO Power 3.3v	
13	PB12	I/O	24	GPIO	AMUX2R: Simulator Channel2 Right; NFCRX: NFC Data In Touch7: Touch Input Channel 7; ADC11: ADC Input Channel 11; SPI1DOA: SPI1 Data Out(A); SD0CLKB:SD0 Clk(B);
14	PB11	I/O	24	GPIO	AMUX2L : Simulator Channel2 Left; NFCTX: NFC Data Out Touch6: Touch Input Channel 6; ADC10: ADC Input Channel 10; SPI1CLKA: SPI1 Clk(A); SD0CMDB: SD0 Command(B); Wakeup13: Port Interrupt /Wakeup 13;
15	PB10	I/O	24	GPIO	UART2RXC: Uart2 Data In(C); Touch5: Touch Input Channel 5; ADC9: ADC Input Channel 9; SPI1_DIA: SPI1 Data In(A); SD0DAT0B: SD0 Data0(B); CAP0: Timer0 Capture;
16	PB9	I/O	24	GPIO	UART2TXC: Uart2 Data Out(C); ADC8: ADC Input Channel 8; CLKOUT1: Clk Out1; SD0DAT1B: SD0 Data1(B); Wakeup12: Port Interrupt /Wakeup 12;
17	VSSIO	P	/	Ground	
18	LDO_IN	P	/	LDO Power Supply	
19	BT_AVDD	P	/	Power 1.5v	
20	VSS2	P	/	Ground	
21	BT_RF	P	/		
22	VSS1	P	/	Ground	
23	BT_OSCI	I	/	OSC In	
24	BT_OSCO	O	/	OSC Out	

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二、电气特性

2.1 PMU 电压、电流特性

表 2-1

符号	参数	最小	典型	最大	单位	测试条件
LDOIN	Voltage Input	3	3.7	5.5	V	
V _{3.3}	Voltage output	-	3.3	-	V	LDO5V = 5V, 100mA loading
V _{1.2}		-	1.2	-	V	LDO5V = 5V, 50mA loading
V _{1.5}	Voltage output		1.5		V	LDO5V=5V, 100mA loading
V _{DACVDD}	DAC Voltage	-	3.1	-	V	LDO5V = 5V, 10mA loading
I _{L3.3}	Loading current	-	-	150	mA	LDO5V = 5V

2.2 IO 输入、输出高低逻辑特性

表 2-2

IO 输入特性						
符号	参数	最小	典型	最大	单位	测试条件
V _{IL}	Low-Level Input Voltage	-0.3	-	0.3* VDDIO	V	VDDIO = 3.3V
V _{IH}	High-Level Input Voltage	0.7* VDDIO	-	VDDIO+0.3	V	VDDIO = 3.3V
IO 输出特性						
V _{OL}	Low-Level Output Voltage	-	-	0.33	V	VDDIO = 3.3V
V _{OH}	High-Level Output Voltage	2.7	-	-	V	VDDIO = 3.3V

2.3 IO 输出能力、上下拉电阻特性

表 2-3

Port 口	普通输出	强输出	上拉电阻	下拉电阻	备注
PA3、PA4 PB13 PC3~PC5	串接 200 欧电阻（寄存器可控制）	16mA	10K	60K	1、PA3 default pulldown 2、内部上下拉阻抗因工艺波动差异，可能存在±20%的偏差
PB9~PB12	8mA	24mA	10K	60K	
USBDM USBDP	4mA	-	1.5K	15K	

2.4 DAC 特性

参数	最小	典型	最大	单位	测试条件
Frequency Response	20	–	200000	Hz	1KHz/0dB 10Kohm loading With A-Weighted Filter
THD+N	–	-70	–	dB	
S/N	–	90	–	dB	
Crosstalk	–	-86	–	dB	
Output Swing	–	1.08	–	Vrms	
Dynamic Range	–	91	–	dB	1KHz/-60dB 10Kohm loading With A-Weighted Filter
DAC Output Power	–	>11	–	mW	32ohm loading

2.5 ADC 特性

参数	最小	典型	最大	单位	测试条件
Dynamic Range	–	91	–	dB	1KHz/-60dB 10Kohm loading With A-Weighted Filter
S/N	–	90	–	dB	1KHz/-60dB
THD+N	–	-70	–	dB	10Kohm loading
Crosstalk	–	-80	–	dB	With A-Weighted Filter

2.6 BT 特性

表 2-4

参数	最小	典型	最大	单位	测试条件
Maximum Output Power	–	2	–	dBm	–
RMS DEVM	–	5.3	–	%	Maximum output power
PEAK DEVM	–	12	–	%	
99% DEVM	–	8	–	%	
EDR Relative Power	–	-1.4	–	dB	
BDR Sensitivity	–	-84	–	dBm	BER=0.001
EDR Sensitivity	–	-86	–	dBm	BER=0.0001

三、封装

3.1 QSOP24

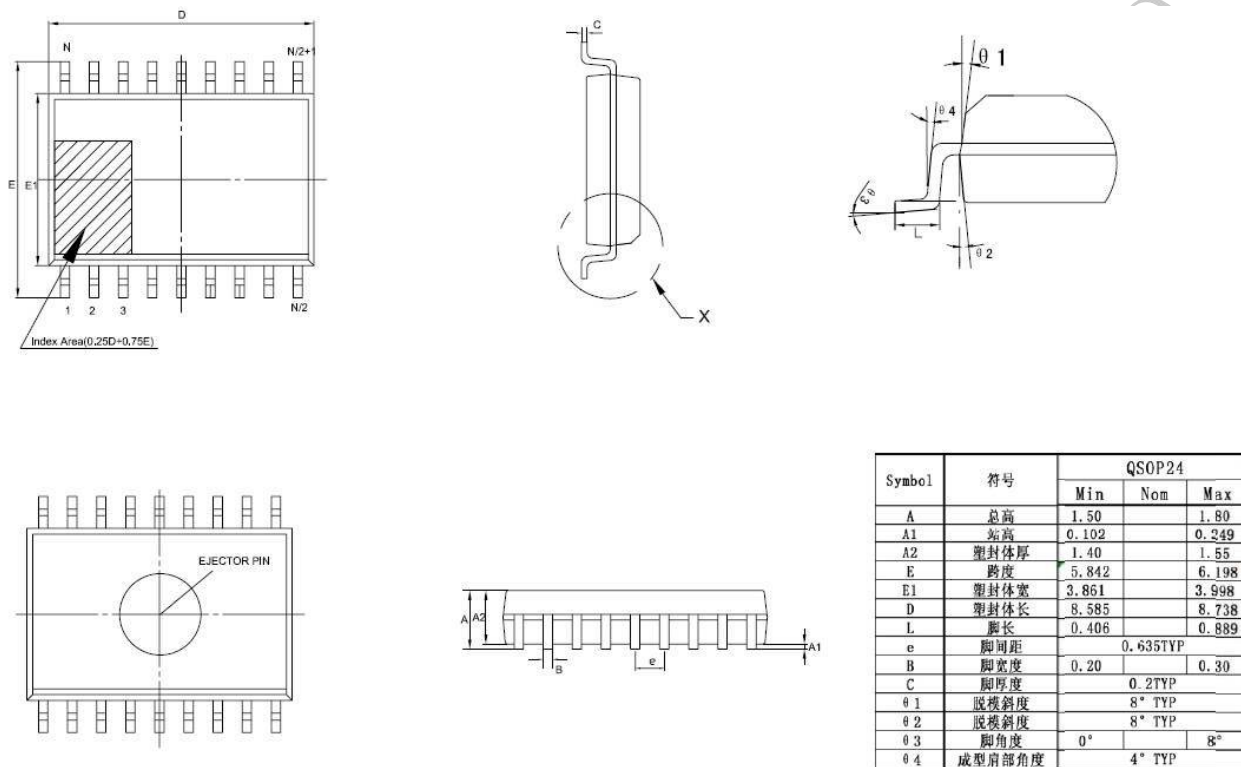


图 3-1 AC6905A_QSOP24 封装图

四、版本信息

日期	版本号	描述
2016.09.12	V1.0	原始版本
2016.12.14	V1.1	升级蓝牙版本为 4.2，增加可支持的蓝牙协议
2016.12.22	V1.2	规范统一蓝牙 4.2 版本格式



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